Table Of Contents

1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges for your telecommunications services. System users are responsible for the security of own system. There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. The manufacturer does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it.
The manufacturer will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the this phone or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on this model must be performed only by the manufacturer or its authorized agent. The user may not make any changes and/or repairs expect as specifically noted in this manual. Therefore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

E. Notice of Radiated Emissions

This model complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

Phone may interfere with sensitive laboratory equipment, medical equipment, etc.Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicated by the sign. Following information is ESD handling:

- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static mat which is also grounded.
- Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

1.3 Abbreviations

For the purposes of this manual, following abbreviations apply:

APC	Automatic Power Control
BB	Baseband
BER	Bit Error Ratio
CC-CV	Constant Current - Constant Voltage
DAC	Digital to Analog Converter
DCS	Digital Communication System
dBm	dB relative to 1 milli watt
DSP	Digital Signal Processing
EEPROM	Electrical Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
FPCB	Flexible Printed Circuit Board
GMSK	Gaussian Minimum Shift Keying
GPIB	General Purpose Interface Bus
GSM	Global System for Mobile Communications
IPUI	International Portable User Identity
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LDO	Low Drop Output
LED	Light Emitting Diode
OPLL	Offset Phase Locked Loop

1. INTRODUCTION

PAM	Power Amplifier Module
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSTN	Public Switched Telephone Network
RF	Radio Frequency
RLR	Receiving Loudness Rating
RMS	Root Mean Square
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SLR	Sending Loudness Rating
SRAM	Static Random Access Memory
PSRAM	Pseudo SRAM
STMR	Side Tone Masking Rating
TA	Travel Adapter
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Control Temperature Compensated Crystal Oscillator
WAP	Wireless Application Protocol

2. PERFORMANCE

2.1 H/W Features

Item	Feature	Comment
Standard Battery	Li-Poly, 600mAh Battery Size : 36 (W) × 24(H) × 6.5(T) [mm] Battery Weight : TBD	
Stand by Current	Under the minimum current consumption environment (such as paging period 9), the level of standby current is below 4mA.	
Talk time	Up to 2 hours (GSM TX Level 5)	
Stand by time	Up to 200 hours (Paging Period: 9, RSSI: -85 dBm)	
Charging time	Approx. Under 3.00 hours	
RX Sensitivity	GSM, EGSM: -104dBm, DCS: -104dBm	
TX output power	GSM, EGSM : 33dBm(Level 5), DCS, PCS : 30dBm(Level 0)	
GPRS compatibility	Class 10	
SIM card type	3V Small Only	
Display	LCD : TFT 176 × 220 pixel 260K Color	
Status Indicator	Hard icons. Key Pad 0 ~ 9, #, *, Menu Key, Confirm Key, Shot Key Send Key, END/PWR Key, Left, Right, Up, Down Key Soft Key(Left/Right), Hot Key(Left/Right)	
ANT	Internal	
EAR Phone Jack	Yes (stereo)	
PC Synchronization	Yes	
Speech coding	EFR/FR/HR	
Data and Fax	Yes	
Vibrator	Yes	
Loud Speaker	Yes	
Voice Recoding	Yes	
Microphone	Yes	
Speaker/Receiver	Speaker/Receiver	
Travel Adapter	Yes	
MIDI	64 Poly (Stereo SPK)	
MP3/AAC	Yes	
Options	Data Cable	

2.2 Technical Specification

<table>
<tr><th>Item</th><th>Description</th><th colspan="6">Specification</th></tr>
<tr><td>1</td><td>Frequency Band</td><td colspan="6">EGSM
• TX: 890 + (n-1024) x 0.2 MHz
• RX: 935 + (n-1024) x 0.2 MHz (n=975~1024)
DCS
• TX: 1710 + (n-512) x 0.2 MHz
• RX: 1805 + (n-512) x 0.2 MHz (n=512~885)
PCS
• TX: 1810 + (n-512) x 0.2 MHz
• RX: 1905 + (n-512) x 0.2 MHz (n=512~885)</td></tr>
<tr><td>2</td><td>Phase Error</td><td colspan="6">RMS < 5 degrees
Peak < 20 degrees</td></tr>
<tr><td>3</td><td>Frequency Error</td><td colspan="6">< 0.1 ppm</td></tr>
<tr><td rowspan="20">4</td><td rowspan="20">Power Level</td><td colspan="6">GSM, EGSM</td></tr>
<tr><td>Level</td><td>Power</td><td>Toler.</td><td>Level</td><td>Power</td><td>Toler.</td></tr>
<tr><td>5</td><td>33 dBm</td><td>±2dB</td><td>13</td><td>17 dBm</td><td>±3dB</td></tr>
<tr><td>6</td><td>31 dBm</td><td>±3dB</td><td>14</td><td>15 dBm</td><td>±3dB</td></tr>
<tr><td>7</td><td>29 dBm</td><td>±3dB</td><td>15</td><td>13 dBm</td><td>±3dB</td></tr>
<tr><td>8</td><td>27 dBm</td><td>±3dB</td><td>16</td><td>11 dBm</td><td>±5dB</td></tr>
<tr><td>9</td><td>25 dBm</td><td>±3dB</td><td>17</td><td>9 dBm</td><td>±5dB</td></tr>
<tr><td>10</td><td>23 dBm</td><td>±3dB</td><td>18</td><td>7 dBm</td><td>±5dB</td></tr>
<tr><td>11</td><td>21 dBm</td><td>±3dB</td><td>19</td><td>5 dBm</td><td>±5dB</td></tr>
<tr><td>12</td><td>19 dBm</td><td>±3dB</td><td></td><td></td><td></td></tr>
<tr><td colspan="6">DCS, PCS</td></tr>
<tr><td>Level</td><td>Power</td><td>Toler.</td><td>Level</td><td>Power</td><td>Toler.</td></tr>
<tr><td>0</td><td>30 dBm</td><td>±2dB</td><td>8</td><td>14 dBm</td><td>±3dB</td></tr>
<tr><td>1</td><td>28 dBm</td><td>±3dB</td><td>9</td><td>12 dBm</td><td>±4dB</td></tr>
<tr><td>2</td><td>26 dBm</td><td>±3dB</td><td>10</td><td>10 dBm</td><td>±4dB</td></tr>
<tr><td>3</td><td>24 dBm</td><td>±3dB</td><td>11</td><td>8 dBm</td><td>±4dB</td></tr>
<tr><td>4</td><td>22 dBm</td><td>±3dB</td><td>12</td><td>6 dBm</td><td>±4dB</td></tr>
<tr><td>5</td><td>20 dBm</td><td>±3dB</td><td>13</td><td>4 dBm</td><td>±4dB</td></tr>
<tr><td>6</td><td>18 dBm</td><td>±3dB</td><td>14</td><td>2 dBm</td><td>±5dB</td></tr>
<tr><td>7</td><td>16 dBm</td><td>±3dB</td><td>15</td><td>0 dBm</td><td>±5dB</td></tr>
</table>

Item	Description	Specification	
5	Output RF Spectrum (due to modulation)	**GSM, EGSM**	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-63
		3,000~ <6,000	-65
		6,000	-71
		DCS, PCS	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-65
		3,000~ <6,000	-65
		6,000	-73
6	Output RF Spectrum (due to switching transient)	**GSM, EGSM**	
		Offset from Carrier (kHz)	Max. (dBm)
		400	-19
		600	-21
		1,200	-21
		1,800	-24

2. PERFORMANCE

<table>
<tr><th>Item</th><th>Description</th><th colspan="3">Specification</th></tr>
<tr><td rowspan="6">6</td><td rowspan="6">Output RF Spectrum
(due to switching transient)</td><td colspan="2">DCS, PCS</td><td></td></tr>
<tr><td colspan="2">Offset from Carrier (kHz).</td><td>Max. (dBm)</td></tr>
<tr><td colspan="2">400</td><td>-22</td></tr>
<tr><td colspan="2">600</td><td>-24</td></tr>
<tr><td colspan="2">1,200</td><td>-24</td></tr>
<tr><td colspan="2">1,800</td><td>-27</td></tr>
<tr><td>7</td><td>Spurious Emissions</td><td colspan="3">Conduction, Emission Status</td></tr>
<tr><td>8</td><td>Bit Error Ratio</td><td colspan="3">GSM, EGSM
BER (Class II) < 2.439% @-102 dBm
DCS, PCS
BER (Class II) < 2.439% @-100 dBm</td></tr>
<tr><td>9</td><td>RX Level Report Accuracy</td><td colspan="3">±3 dB</td></tr>
<tr><td>10</td><td>SLR</td><td colspan="3">8 ±3 dB</td></tr>
<tr><td rowspan="10">11</td><td rowspan="10">Sending Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>-</td></tr>
<tr><td>200</td><td>0</td><td>-</td></tr>
<tr><td>300</td><td>0</td><td>-12</td></tr>
<tr><td>1,000</td><td>0</td><td>-6</td></tr>
<tr><td>2,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,400</td><td>4</td><td>-9</td></tr>
<tr><td>4,000</td><td>0</td><td>-</td></tr>
<tr><td>12</td><td>RLR</td><td colspan="3">2 ±3 dB</td></tr>
<tr><td rowspan="11">13</td><td rowspan="11">Receiving Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>-</td></tr>
<tr><td>200</td><td>0</td><td>-</td></tr>
<tr><td>300</td><td>2</td><td>-7</td></tr>
<tr><td>500</td><td>*</td><td>-5</td></tr>
<tr><td>1,000</td><td>0</td><td>-5</td></tr>
<tr><td>3,000</td><td>2</td><td>-5</td></tr>
<tr><td>3,400</td><td>2</td><td>-10</td></tr>
<tr><td>4,000</td><td>2</td><td></td></tr>
<tr><td colspan="3">* Mean that Adopt a straight line in between 300 Hz and 1,000 Hz to be Max. level in the range.</td></tr>
</table>

Item	Description	Specification	
14	STMR	13 ±5 dB	
15	Stability Margin	> 6 dB	
16	Distortion	dB to ARL (dB)	Level Ratio (dB)
		-35	17.5
		-30	22.5
		-20	30.7
		-10	33.3
		0	33.7
		7	31.7
		10	25.5
17	Side Tone Distortion	Three stage distortion < 10%	
18	System frequency (13 MHz) tolerance	≤ 2.5ppm	
19	32.768KHz tolerance	≤ 30ppm	
20	Ringer Volume	At least 65 dBspl under below conditions: 1. Ringer set as ringer. 2. Test distance set as 50 cm	
21	Charge Current	Fast Charge : < 440 mA Slow Charge : < 66 mA	
22	Antenna Display	Antenna Bar Number	Power
		5	-85 dBm ~
		4	-90 dBm ~ -86 dBm
		3	-95 dBm ~ -91 dBm
		2	-100 dBm ~ -96 dBm
		1	-105 dBm ~ -101 dBm
		0	~ -105 dBm
23	Battery Indicator	Battery Bar Number	Voltage
		0	3.36 ~ 3.54 V
		1	3.55 ~ 3.66 V
		2	3.67 ~ 3.72 V
		3	3.73 ~ 3.84 V
		4	3.85 V ~
24	Low Voltage Warning	3.55 ±0.03V (Call)	
		3.48 ±0.03V (Standby)	

2. PERFORMANCE

Item	Description	Specification
25	Forced shut down Voltage	3.35±0.03 V
26	Battery Type	1 Li-Poly Battery Standard Voltage = 3.7 V Battery full charge voltage = 4.2 V Capacity: 800mAh
27	Travel Charger	Switching-mode charger Input: 100 ~ 240 V, 50/60 Hz Output: 5.2 V, 800 mA

3. TECHNICAL BRIEF

3.1 Transceiver (SI4210, U401)

The RF parts consist of a transmitter part, a receiver part, a digitally-controlled crystal oscillator. The Aero® II transceiver is a complete RF front end for multi-band GSM and GPRS wireless communications. The receive section interfaces between the RF band-select SAW filters and the baseband subsystem. The Aero II receiver leverages a proven digital low-IF architecture and enables a universal baseband interface without the need for complex dc offset compensation. The transmit section of Aero II provides a complete upconversion path from the baseband subsystem to the power amplifier (PA) using an offset phase-locked loop (OPLL) integrated with Silicon Laboratories' patented synthesizer technology. All sensitive components, such as TX/RF VCOs, loop filters, tuning inductors, and varactors are completely integrated into a single integrated circuit. The Aero II transceiver includes a digitallycontrolled crystal oscillator (DCXO) and completely integrates the reference oscillator and varactor functionality.

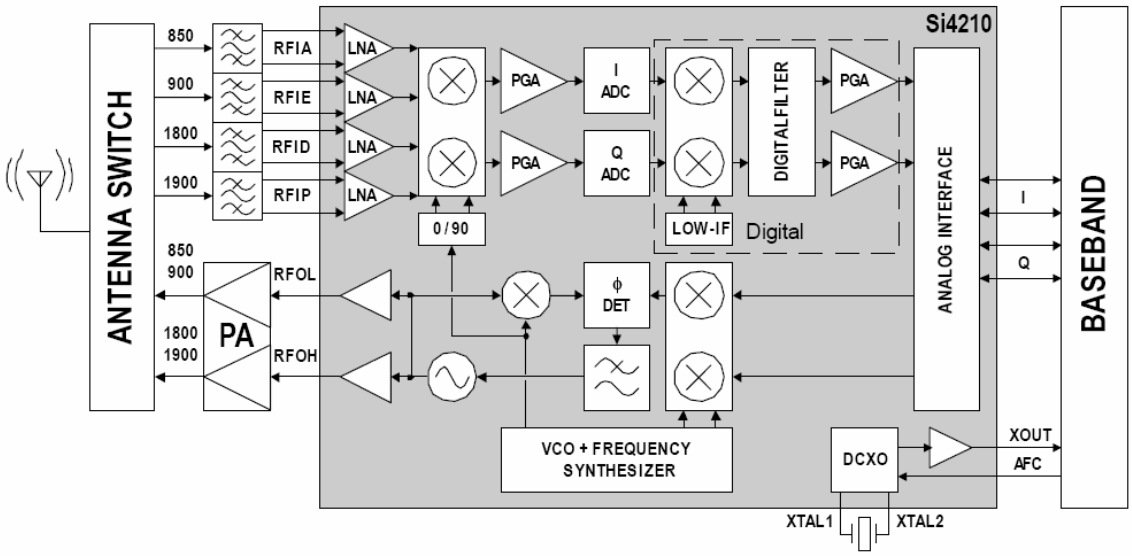


Figure. 3-1 SI4210 TRANSCEIVER BLOCK DIAGRAM

3. TECHNICAL BRIEF

(1) Receiver Part

The Aero II transceiver uses a digital low-IF receiver architecture that allows for the on-chip integration of the channel selection filters, eliminating the external RF image reject filters, and the IF SAW filter required in conventional superheterodyne architectures. Compared with direct-conversion architectures, the digital low-IF architecture has a much greater degree of immunity to dc offsets that can arise from RF local oscillator (RFLO) self-mixing, second-order distortion of blockers (AM suppression), and device 1/f noise.

The digital low-IF receiver's immunity to dc offsets has the benefit of expanding part selection and improving manufacturing. At the front end, the common-mode balance requirements on the input SAW filters are relaxed, and the PCB board design is simplified. At the radio's opposite end, the BBIC is one of the handset's largest BOM contributors. It is not uncommon for a direct conversion solution to be compatible only with a BBIC from the same supplier in order to address the complex dc offset issues. However, since the Aero II transceiver has no requirement for BBIC support of complex dc offset compensation, it is able to interface to all of the industry leading baseband ICs.

The receive (RX) section integrates four differential input low noise amplifiers (LNAs) supporting the GSM 850 (869-894 MHz), E-GSM 900 (925-960 MHz), DCS 1800 (1805-1880 MHz), and PCS 1900 (1930-1990 MHz) bands. The LNA inputs are matched to 150 or 200 balanced-output SAW filters through external LC matching networks. See “AN150: Aero II Transceiver PCB Design Guide” for implementation details. The active LNA input is automatically selected by the ARFCN[9:0] bits and the BANDIND bit in Register 21h. If performing LNA swapping, the LNASWAP bit in Register 05h is also needed. Please refer to section 4.1.1 for details. The LNA gain is controlled with the LNAG bit in Register 20h.

A quadrature image-reject mixer downconverts the RF signal to a low intermediate frequency (IF). The mixer output is amplified with an analog programmable gain amplifier (PGA) that is controlled with the AGAIN[2:0] bits in Register 20h. The quadrature IF signal is digitized with high resolution analog-todigital converters (ADCs).

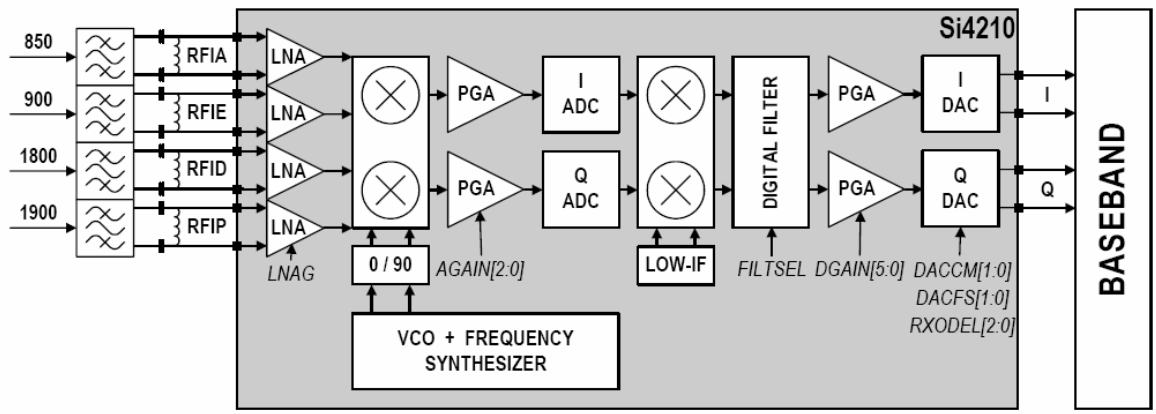


Figure. 3-2 SI4210 RECEIVER PART

The ADC output is downconverted to baseband with a digital quadrature local oscillator signal. Digital decimation and FIR filters perform digital filtering, and remove ADC quantization noise, blockers, and reference interferers. The response of the FIR filter is programmable to a flat pass band setting (FILTSEL = 0, Register 08h) and a linear phase setting (FILTSEL = 1, Register 08h). After filtering, the digital output is scaled with a PGA, which is controlled with the DGAIN[5:0] bits in Register 20h.

The LNAG, AGAIN[2:0], and DGAIN[5:0] register bits should be set to provide a constant amplitude signal to the baseband receive inputs. See “AN153: Aero II Transceiver AGC Strategy” for more details. Digitalto-analog converters (DACs) drive differential I and Q analog signals onto the BIP, BIN, BQP, and BQN pins to interface to standard analog-input baseband ICs.

The receive DACs are updated at 1.083 MHz and have a first-order reconstruction filter with a 1 MHz bandwidth. No special processing is required in the baseband for dc offset compensation. The receive and transmit baseband I/Q pins are multiplexed together in a 4-wire interface (BIP, BIN, BQP, and BQN). The common mode level at the receive I and Q outputs is programmable with the DACCM[1:0] bits, and the full scale level is programmable with the DACFS[1:0] bits in Register 05h.

(2) Transmit section

The transmit section consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL), and two 50 Ω output buffers that can drive an external power amplifier (PA). One output is for the GSM 850 (824-849 MHz) and E-GSM 900 (880-915 MHz) bands and one output is for the DCS 1800 (1710-1785 MHz) and PCS 1900 (1850-1910 MHz) bands.

The OPLL requires no external filtering to attenuate transmitter noise and spurious signals in the receive band, saving both cost and power. The output of the transmit VCO (TXVCO) is a constant-envelope signal that reduces the problem of spectral spreading caused by non-linearity in the PA. Additionally, the TXVCO benefits from isolation provided by the transmit output buffers. This significantly minimizes any load pull effects and eliminates the need for off-chip isolation networks.

A quadrature mixer upconverts the differential in-phase (BIP, BIN) and quadrature (BQP, BQN) baseband signals to an intermediate frequency (IF) that is filtered and which is used as the reference input to the OPLL. The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO. Low-pass filters before the OPLL phase detector reduce the harmonic content of the quadrature modulator and feedback mixer outputs.

The transmit I/Q interface must have a non-zero input no later than 94 quarter bits after PDN is asserted for proper operation. If the baseband is unable to provide a sufficient TX I/Q non-zero input preamble, then the CWDUR bits in Register 05h can be used to provide a preamble extension.

The receive and transmit baseband I/Q pins are multiplexed together in a 4-wire interface (BIP, BIN, BQP, and BQN). In transmit mode, the BIP, BIN, BQP, and BQN pins provide the analog I/Q input from the baseband subsystem. The full-scale level at the baseband input pins is programmable with the BBG[1:0] bits in Register 05h. The I and Q signals are automatically swapped within the Aero II transceiver when switching bands. The transmit output path is automatically selected by the ARFCN[9:0] bits and the BANDIND bits in Register 21h. As an option for multislot applications, direct control of the output transmit buffers during a burst is offered through the PDTXO bit in Register 23h.

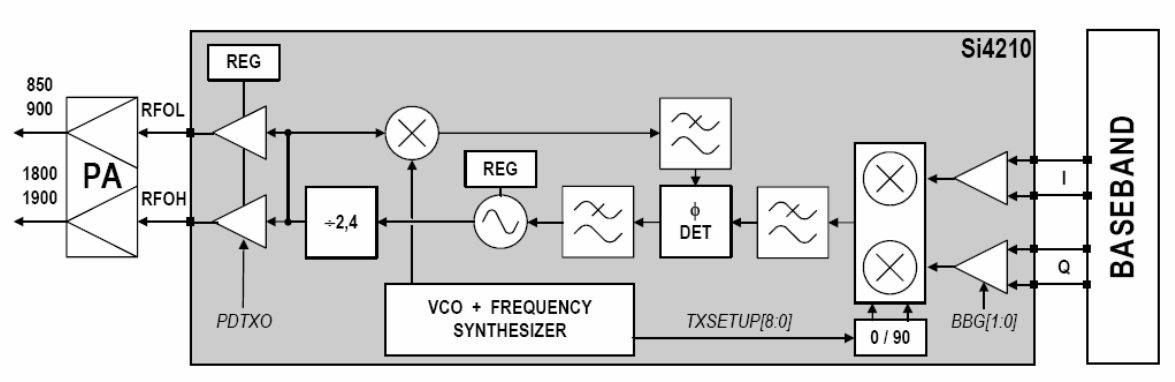


Figure. 3-3 SI4210 TRANSMITTER PART

(3) Digitally-controlled crystal oscillator

The Aero II transceiver integrates the DCXO circuitry required to generate a precise system reference clock using only an external crystal resonator. The DCXO replaces a discrete VC-TCXO module. The DCXO allows for the use of a standard 26 MHz crystal, which reduces both cost and area compared to using a VCTCXO module. There are no external varactors or trim capacitors required. This simplifies the design, programming, and manufacturing compared to less integrated solutions.

The DCXO uses the CDAC and CAFC arrays to correct for both static and dynamic frequency errors, respectively. An internally digitally programmable capacitor array (CDAC) provides a coarse method of adjusting the reference frequency in discrete steps. The CDAC[6:0] bits in Register 03h are programmed to compensate for static variations in PCB design, manufacturing, and crystal tolerance, and are typically set to center the oscillator frequency during production. A second capacitor array (CAFC) allows for fine and continuous dynamic adjustment of the reference frequency by an external control voltage (AFC). This control voltage is supplied by the AFC DAC of the baseband and should be connected to the transceiver AFC pin (pin 27). The baseband determines the appropriate frequency adjustment based on the receipt of the FCCH burst. The baseband then adjusts the AFC voltage to correct for frequency variations caused by temperature drift.

The transceiver can be adjusted for the corresponding baseband AFC input full-scale voltage by setting the AFCREF bit in Register 04h. Additionally, the Aero II transceiver supports an optional Digital AFC mode for DCXO operation that is selected by the AFCC bit in Register 04h. In digital mode, the connection between the baseband and transceiver is eliminated. AFC control is performed directly by a register write operation. This has the benefit of further easing PCB design and enabling a DAC in the baseband to be allocated to another function.

The Aero II transceiver can be configured in DCXO mode or VC-TCXO mode by the XMODE pin. To use the transceiver in DCXO mode, the XMODE pin is tied high. The XTAL1 and XTAL2 pins are then connected directly to the 26 MHz crystal. No additional components are required. The use of an external VCTCXO module is also supported by tying the XMODE pin low. The VC-TCXO output should be input into XTAL1, and XTAL2 should be tied low.

A buffer is available to provide a reference clock output from the XOUT pin to the baseband input. The XOUT buffer is enabled when the XEN pin is set high, independent of the PDN pin. To achieve complete powerdown during sleep, the XEN pin should be set low to disable the XOUT buffer. The XOUT buffer is specified to drive a maximum load of 10 pF. The reference clock should be set to 13 MHz or 26 MHz by the XDIV pin. When XDIV is tied low, XOUT is 26 MHz, and when it is tied high, XOUT is 13 MHz.

For a simple to follow methodology and detailed instructions on crystal selection, see "AN152: Selecting a Crystal for Aero II Designs," or contact Silicon Laboratories Applications Support for assistance.

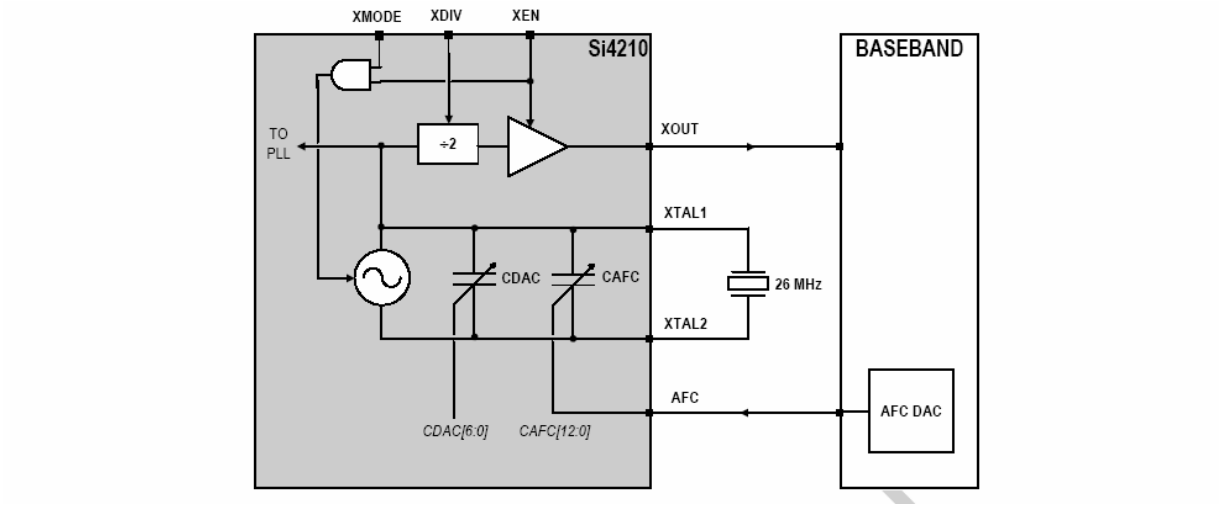


Figure. 3-4 DCXO BLOCK DIAGRAM

3.2 Power Amplifier (SKY77328, U400)

The RF parts consist of a transmitter part, a receiver part, a frequency synthesizer part, a voltage supply part, and a VCTCXO part.

The SKY77328 Power Amplifier Module (PAM) is designed in a low profile (1.2 mm), compact form factor for quad-band cellular handsets comprising GSM850/900, DCS1800, and PCS1900 operation. The PAM also supports Class 12 General Packet Radio Service (GPRS) multi-slot operation. The module consists of separate GSM850/900 PA and DCS1800/PCS1900 PA blocks, impedance-matching circuitry for 50 Ω input and output impedances, and a Power Amplifier Control (PAC) block with an internal current-sense resistor. The custom BiCMOS integrated circuit provides the internal PAC function and interface circuitry. Fabricated onto a single Gallium Arsenide (GaAs) die, one Heterojunction Bipolar Transistor (HBT) PA block supports the GSM850/900 bands and the other supports the DCS1800 and PCS1900 bands. Both PA blocks share common power supply pins to distribute current. The GaAs die, the Silicon (Si) die, and the passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold. RF input and output ports of the SKY77328 are internally matched to a 50 Ω load to reduce the number of external components for a quad-band design. Extremely low leakage current (2.5 μA, typical) of the dual PA module maximizes handset standby time. The SKY77328 also contains band-select switching circuitry to select GSM (logic 0) or DCS/PCS (logic 1) as determined from the Band Select (BS) signal. In Figure 1 below, the BS pin selects the PA output (DCS/PCS OUT or GSM850/900 OUT) and the Analog Power Control (VAPC) controls the level of output power. The VBATT pin connects to an internal current-sense resistor and interfaces to an integrated power amplifier control (iPAC™) function, which is insensitive to variations in temperature, power supply, process, and input power. The ENABLE input allows initial turn-on of PAM circuitry to minimize battery drain.

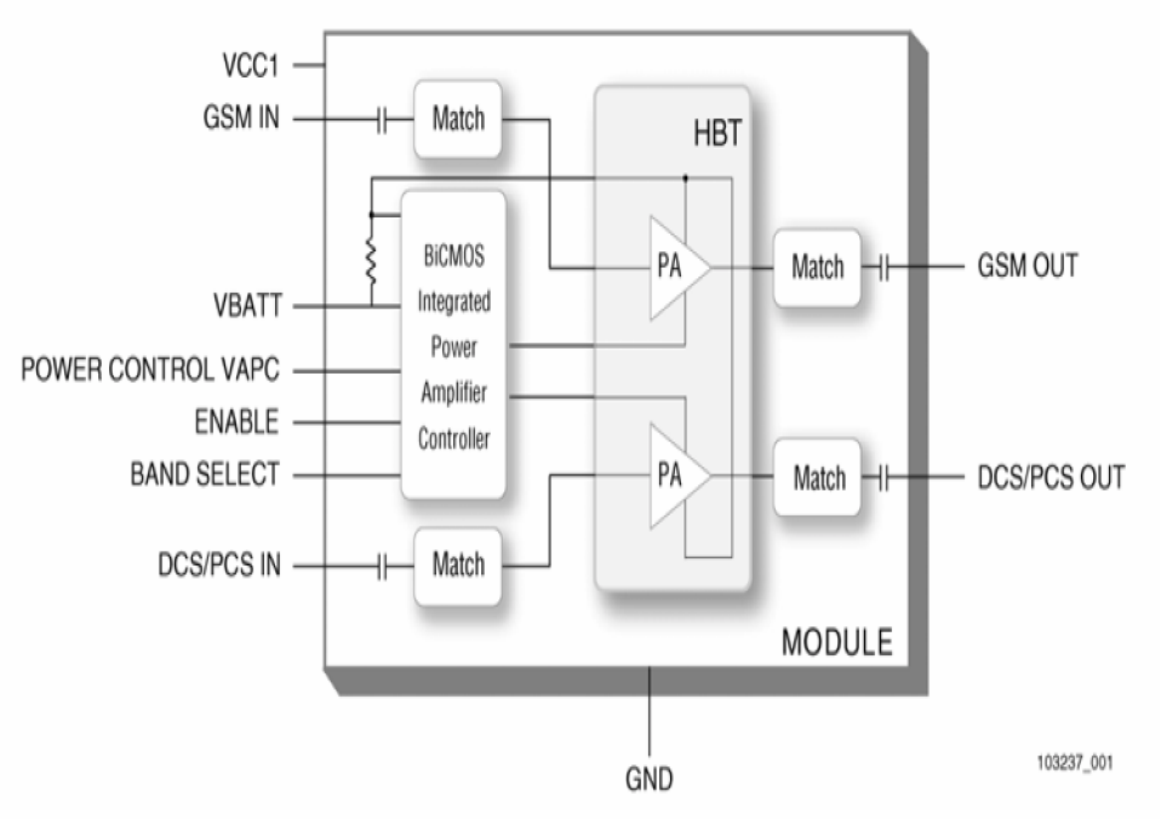


Figure. 3-5 SKY77328 FUNCTIONAL BLOCK DIAGRAM

3.3 26 MHz Clock (VCTCXO, X400)

The 26 MHz clock(X501) consists of a TCXO(Temperature Compensated Crystal Oscillator) which oscillates at a frequency of 26 MHz. It is used within the SI4210, analog base band chipset (U101, AD6535ABCZ), digital base band chipset (U102, AD6527BABCZ).

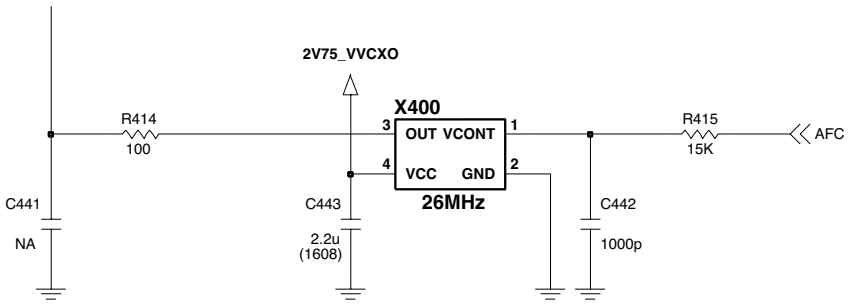


Figure 3-6 VCTCXO CIRCUIT DIAGRAM

3.4 FEM for Triband(FL400)

Select Mode	Vc(EGSM)	Vc(DCS/PCS)
EGSM-Rx	Low	Low
EGSM-Tx	High	Low
DCS-Rx	Low	Low
PCS-Rx	Low	Low
DCS/PCS-Tx	Low	High

Table 3-1 FEM CONTROL LOGIC

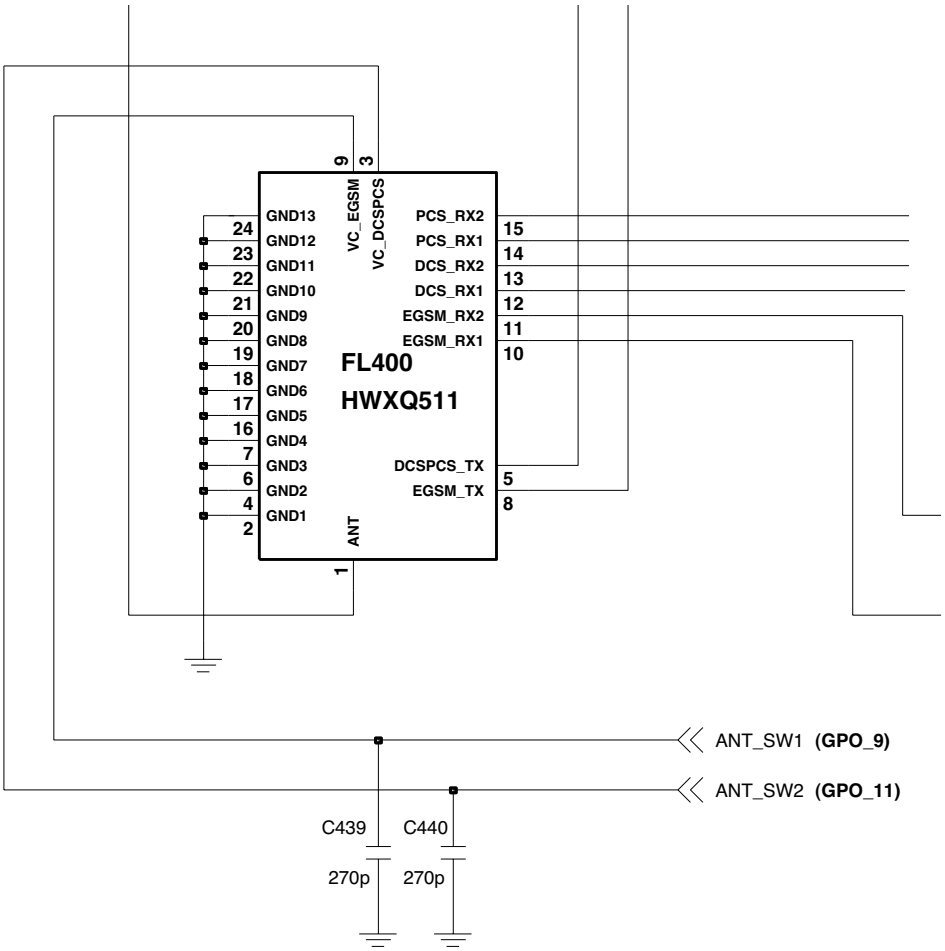


Figure 3-7 FEM CIRCUIT DIAGRAM

3.5 Digital Main Processor (AD6527B, U102)

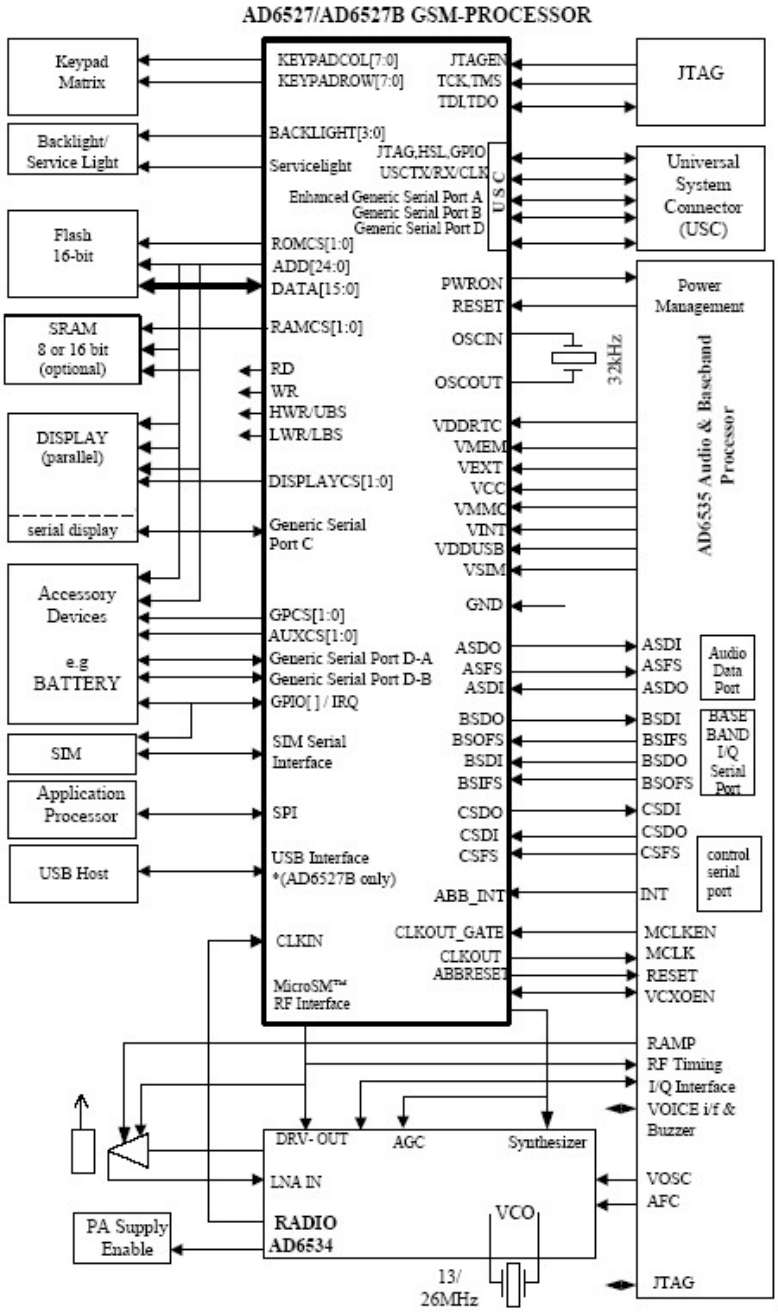


Figure 3-5. SYSTEM INTERCONECTION OF AD6527 EXTERNAL INTERFACE

• AD6527 is an ADI designed processor.

• AD6527 consists of

1. Control Processor Subsystem
   - 32-bit ARM7TDMI Control Processor
   - 58.5 MHz operation at 1.7V
   - On-board 16KB instruction/Data Cache
   - 1 Mbits of on-chip System SRAM

2. DSP Subsystem
   - 16-bit Fixed Point DSP Processor
   - 91 MIPS at 1.7V
   - 16K word Data and 16K word Program SRAM
   - 4K word Program Instruction Cache
   - Architecture supports Full Rate, Enhanced Full Rate, Half Rate, and AMR Speech Encoding/Decoding Algorithms

3. Peripheral Subsystem
   - Shared on-chip peripheral and off-chip interface:
   - Support for Burst and Page Mode Flash
   - Support for Pseudo SRAM
   - Ciphering module for GPRS supporting GAE1 and GAE2 encryption algorithms
   - Parallel and Serial Display Interface
   - 8 x 8 Keypad Interface
   - Four independent programmable backlight plus One Service Light
   - 1.8V and 3.0V, 64 kbps SIM interface
   - Universal System Connector Interface
   - Slow, Medium and Fast IrDA transceiver interface
   - Enhanced Generic Serial Port
   - Dedicated SPI interface
   - Thumbwheel Interface
   - JTAG Interface for Test and In-Circuit Emulation

4. Other
   - Supports 13 MHz and 26 MHz Input Clocks
   - 1.8V Typical Core Operating Voltages
   - 204-Ball LFBGA(mini-BGA) Package

5. Applications
   - GSM900/DCS1800/PCS1900/PCS850 Wireless Terminals
   - GSM Phase 2+ Compliant
   - GPRS Class 12 Compliant
   - Multimedia Services(MMS)
   - Extended Messaging System(EMS)

3.4.1 Interconnection with external devices

A. RTC block interface

Countered by external X-TAL
The X-TAL oscillates 32.768KHz

B. RF interface

The AD6527B control RF parts through PA_BAND, ANT_SW1, ANT_SW2, ANT_SW3 , CLKON , PA_EN, S_EN, S_DATA, S_CLK, RF_PWR_DWN.

Signals	Description
PA_BAND (GPO 17)	PAM Band Select
ANT_SW1 (GPO 9)	Antenna switch Band Select
ANT_SW2 (GPO 11)	Antenna switch Band Select
CLKON	RF LDO Enable/Disable
PA_EN (GPO 16)	PAM Enable/Disable
S_EN (GPO 19)	PLL Enable/Disable
S_DATA (GPO 20)	Serial Data to PLL
S_CLK (GPO 21)	Clock to PLL
RF_PWR_DWN(GPO 4)	Power down Input

Table 3-4. RF CONTROL SIGNALS DESCRIPTION

C. SIM interface

The AD6527B provides SIM Interface Module. The AD6527B checks status periodically during established call mode whether SIM card is inserted or not, but it doesn't check during deep Sleep mode. In order to communicate with SIM card, 3 signals SIM_DATA, SIM_CLK, SIM_RST(GPIO_23) are required. The descriptions about the signals are given by bellow Table 3-6 in detail.

Signals	Description
SIM_DATA	This pin receives and sends data to SIM card. This model can support only 3.0 volt interface SIM card.
SIM_CLK	Clock 3.25MHz frequency.
SIM_RST (GPIO_23)	Reset SIM block

Table 3-5. SIM CONTROL SIGNALS DESCRIPTION

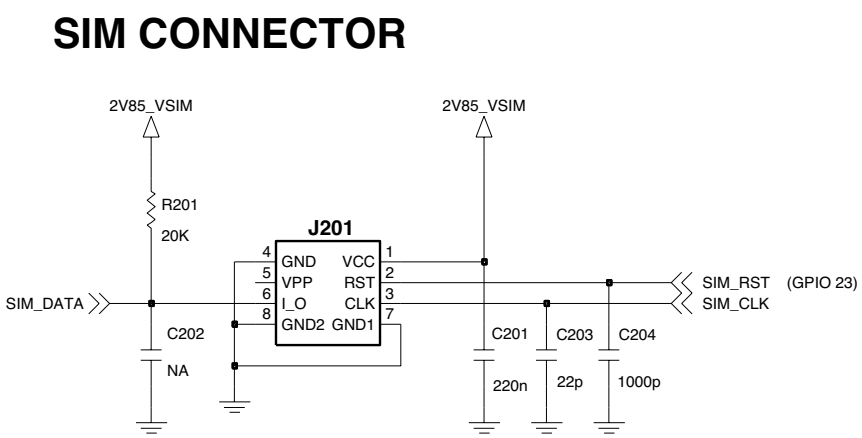


Figure 3-6. SIM Interface of AD6527B

D. Key interface

Include 5 column , 5 row. The AD6527B detects whether key is pressed or not by using interrupt method.

E. AD6535 Interrupt

AD6535 provides an active-high interrupt output signal. Interrupt signals are generated by the Auxiliary ADC, audio, and charger modules.

3.4.2 AD6527B Architecture

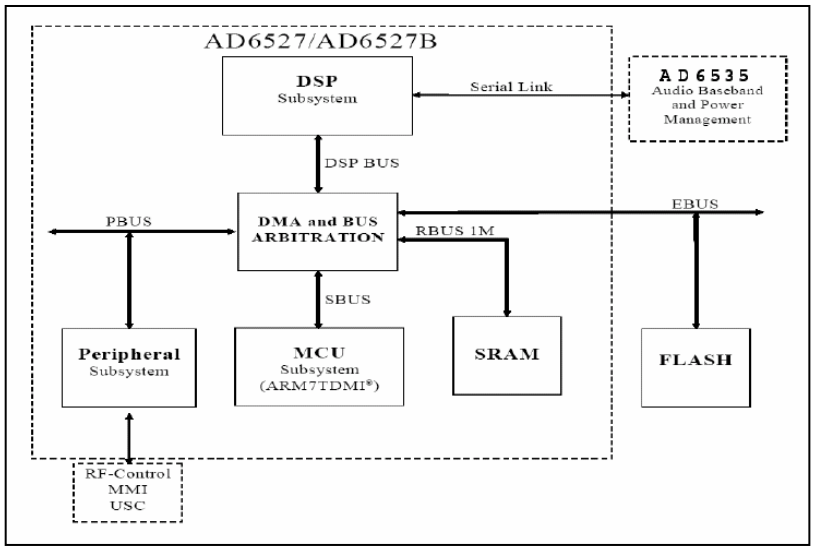


Figure 3-7. AD6527B Architecture

The internal architecture of AD6527B is shown above Figure 3-7. AD6527 regroups three main subsystems connected together through a dynamic and flexible communication bus network. It also includes onboard system RAM (SRAM) and interfaces with external Flash Memory, Baseband converter functions, and terminal functions like MMI, SIM and Universal System Connector (USC).

The Digital Signal Processing (DSP) subsystem primarily hosts all the speech processing, channel equalization and channel codec functions. The code used to implement such functions can be stored in external Flash Memory and dynamically downloaded on demand into the DSP's program RAM and Instruction Cache. The micro-controller subsystem supports all the GSM terminal software, including the layer 1, 2 and 3 of the GSM protocol stack, the MMI, and applications software such as data services, test and maintenance. It is tightly associated with on-chip system SRAM and also includes boot ROM memory with a small dedicated routine to facilitate the initialization of the external Flash Memory via code download using the on-chip serial interface to the external Flash Memory interface. The peripheral subsystem is composed of system peripherals such as interrupt controller, real time clock, watch dog timer, power management and a timing and control module. It also includes peripheral interfaces to the terminal functions: keyboard, battery supervision, radio and display. Both the DSP and the MCU can access the peripheral subsystem via the peripheral bus (PBUS). For program and data storage, both the MCU subsystem and the DSP subsystem can access the on chip system SRAM and external memory such Flash Memory. The access to the SRAM module is made through the RAM Bus (RBUS) under the control of the bus arbitration logic. Similarly, access to the Flash Memory is through the parallel External Bus (EBUS).

3.5 Analog Main & Power Management Processor (AD6535, U101)

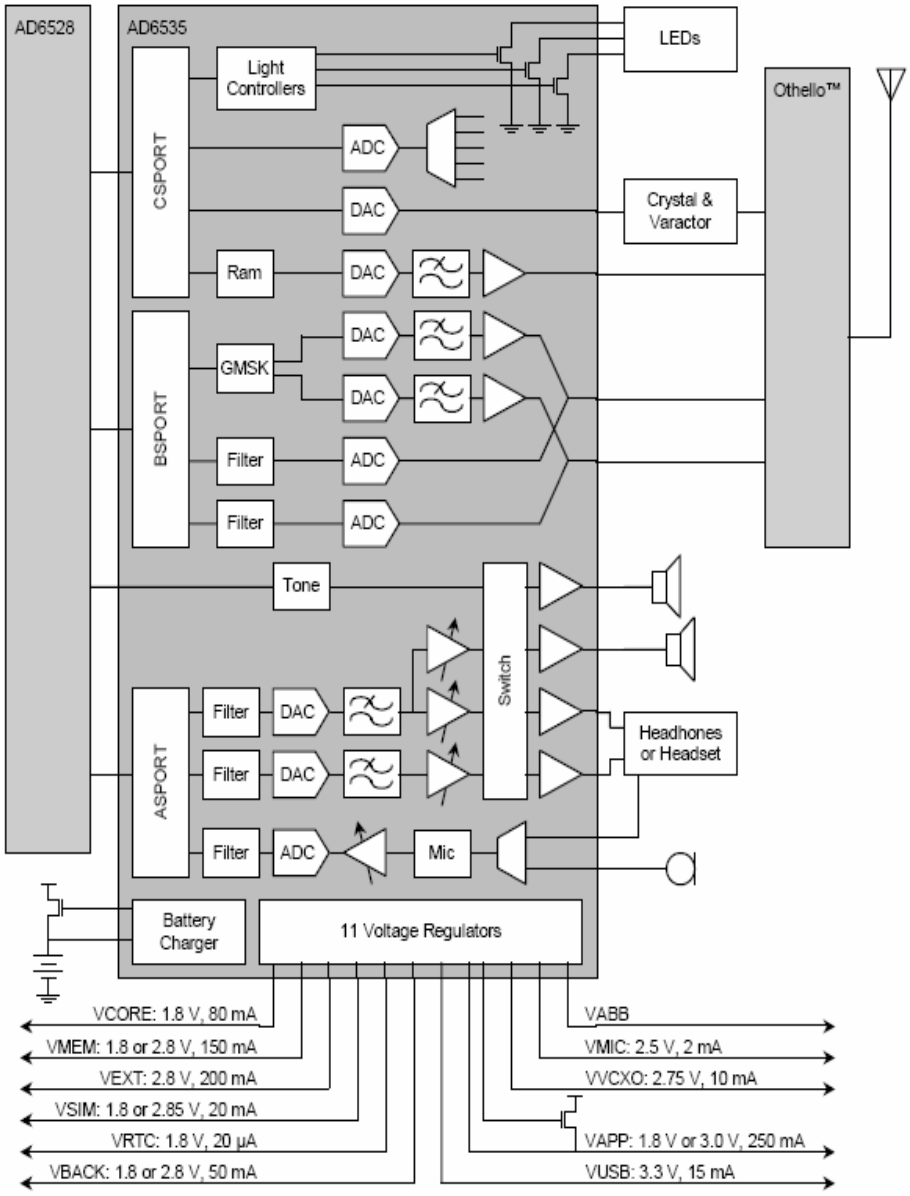


Figure 3-8. AD6535 FUNCTIONAL BLOCK DIAGRAM

3. TECHNICAL BRIEF

• AD6535 is an ADI designed Analog Baseband processor. AD6535 covers the processing GMSK modulation interface, Aux ADC, Voice signal processing and Power Management.

• AD6535 consists of

1. BB Transmit section
   • GMSK Modulation
   • I-channel & Q-channel Transmit DACs and Filters
   • Power Ramping DAC

2. BB Receive section
   • I-channel & Q-channel Receive ADCs and Filters

3. Auxiliary section
   • Voltage Reference
   • Automatic Frequency Control DAC
   • Auxiliary ADC
   • Light Controllers

4. Audio Section
   • 8 kHz & 16 kHz Voiceband Codec
   • 48 kHz Monophonic DAC
   • Power Amplifiers

5. Power Management section
   • Voltage Regulators
   • Battery Charger
   • Battery Protection

6. Digital Processor section
   • Control, Baseband, and Audio Serial Ports
   • Interrupt Logic

3.5.1 Baseband Transmit Section

1. The AD6537B Baseband Transmit Section is designed to support GMSK for both single-slot and multi-slot application.
2. The AD6535 includes a digital GMSK modulator which is used for GSM application. The GMSK modulator uses a ROM lookup table to modulate the serial data stream ffrom the BSPORT. The GMSK modulator is based on 3GPP TS 45.004 ver.5.1.0 Release 5

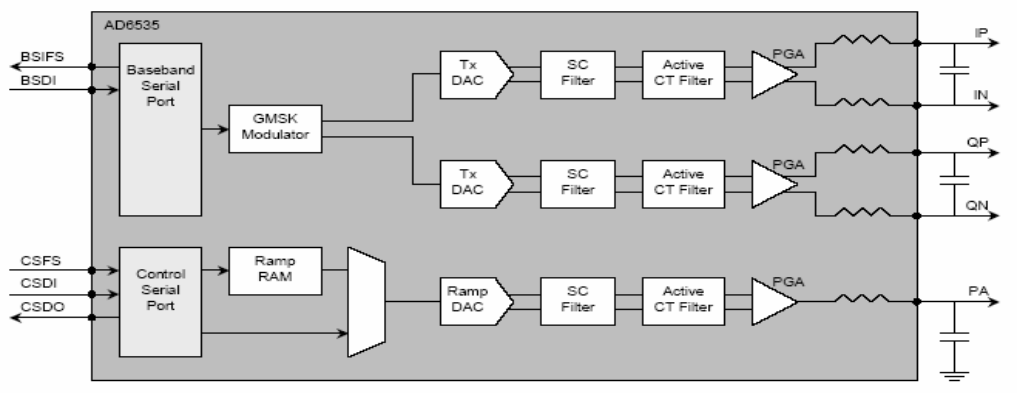


Figure 3-9. AD6535 BASEBAND TRANSMIT SECTION

3.5.2 Baseband Receive Section

1. This section consists of two identical ADC channels that process baseband in-phase(I) and quadrature(Q) input signals.

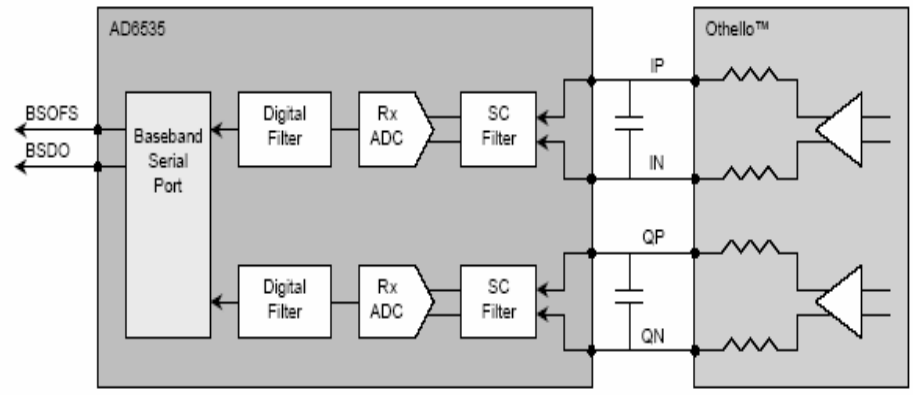


Figure 3-10. AD6535 BASEBAND RECEIVER SECTION

3.5.3 Auxiliary Section

1. This section includes an Automatic Frequency Control(AFC) DAC, voltage reference buffers, an Auxiliary ADC, and light controllers.
   • AFC DAC: 13 bits

2. This section also contains AUX ADC and Voltage Reference
   • IDAC: 10 bits
   • The Auxiliary ADC provides :
     - Two differential inputs for temperature sensing.
     - A differential input for the battery charger current sensor

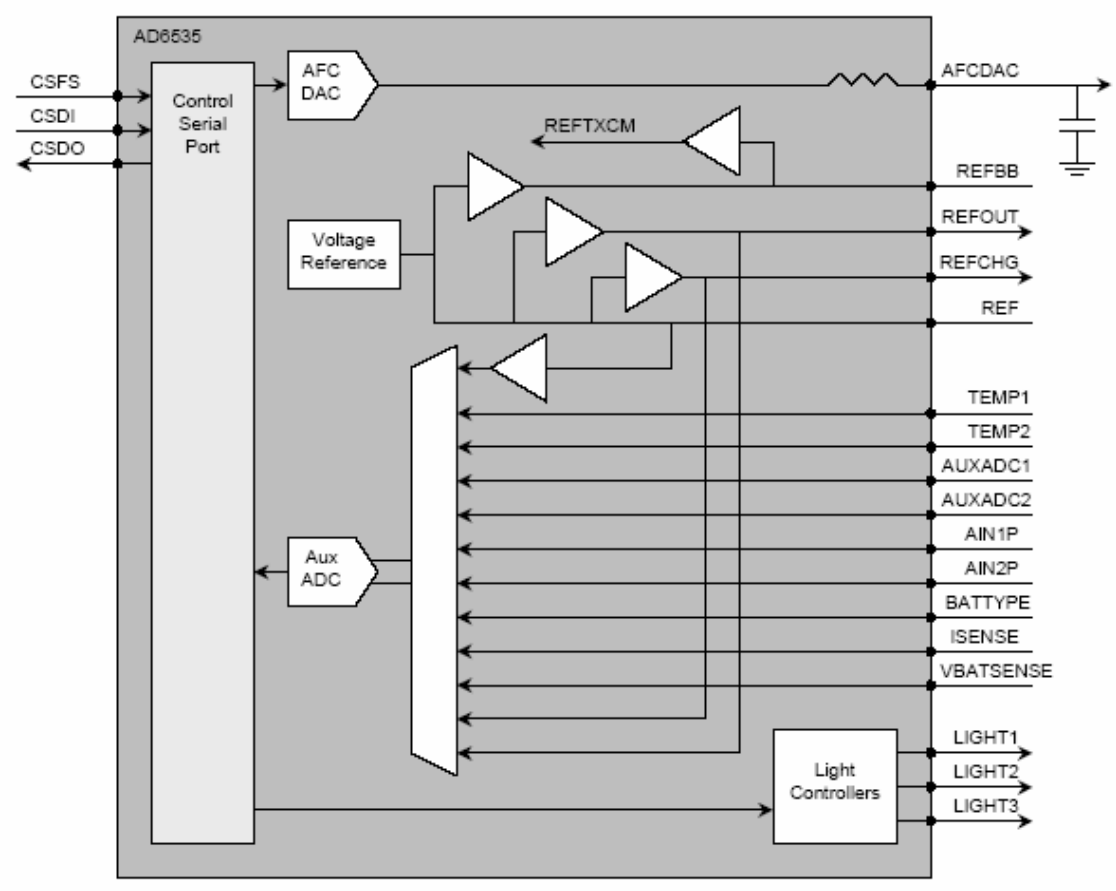


Figure 3-11. AD6535 AUXILIARY SECTION

3.5.4 Audio Section

1. The AD6535 Audio section supports communications and personal audio applications.
2. The Audio Section provides an audio codec with two digital-to-analog converter, a ring tone volume controller, a microphone interface, and analog input and output channels.

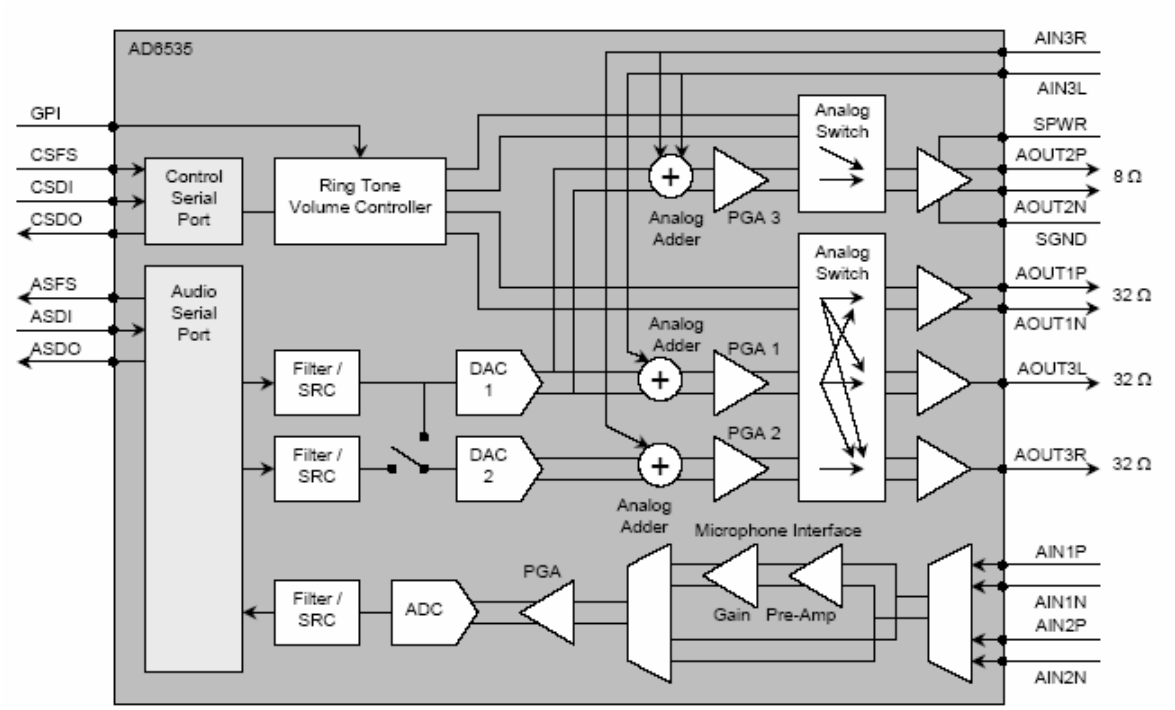


Figure 3-12. AD6535 AUDIO SECTION

3.5.5 Power Management

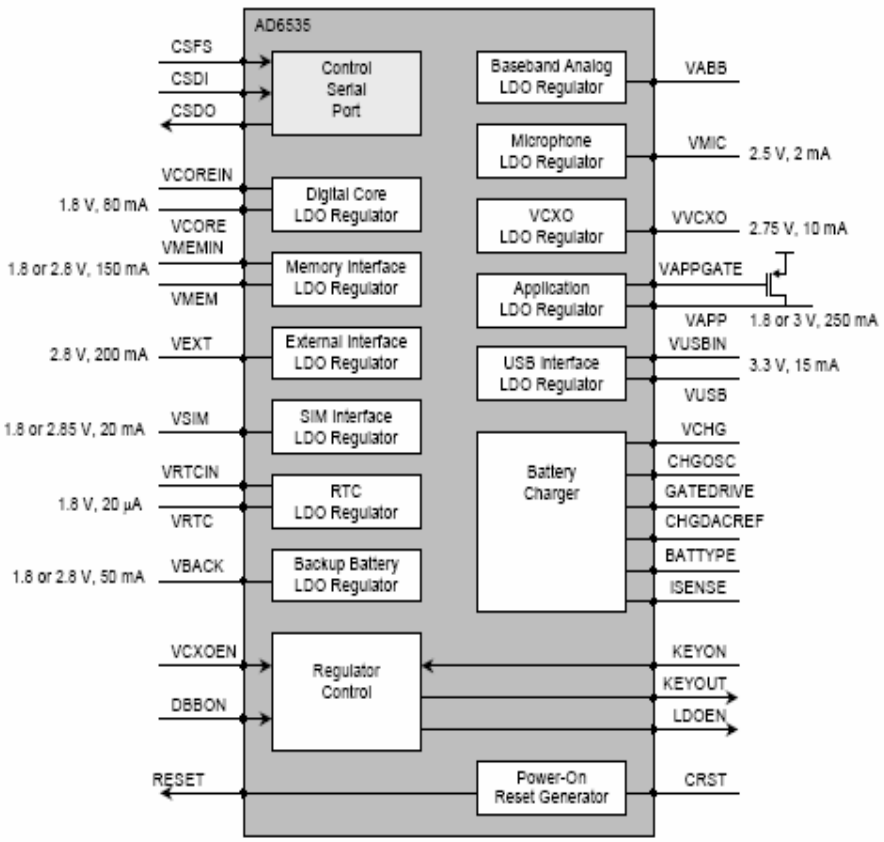


Figure 3-13. AD6535 POWER MANAGEMENT SECTION

1. Power up sequence logic

1. The AD6535 controls power on sequence
2. Power on sequence
   - If a battery is inserted, the battery powers the 8 LDOs.
   - Then if PWRONKEY is detected, the LDOs output turn on.
   - REFOUT is also enabled
   - Reset is generated and send to the AD6527B

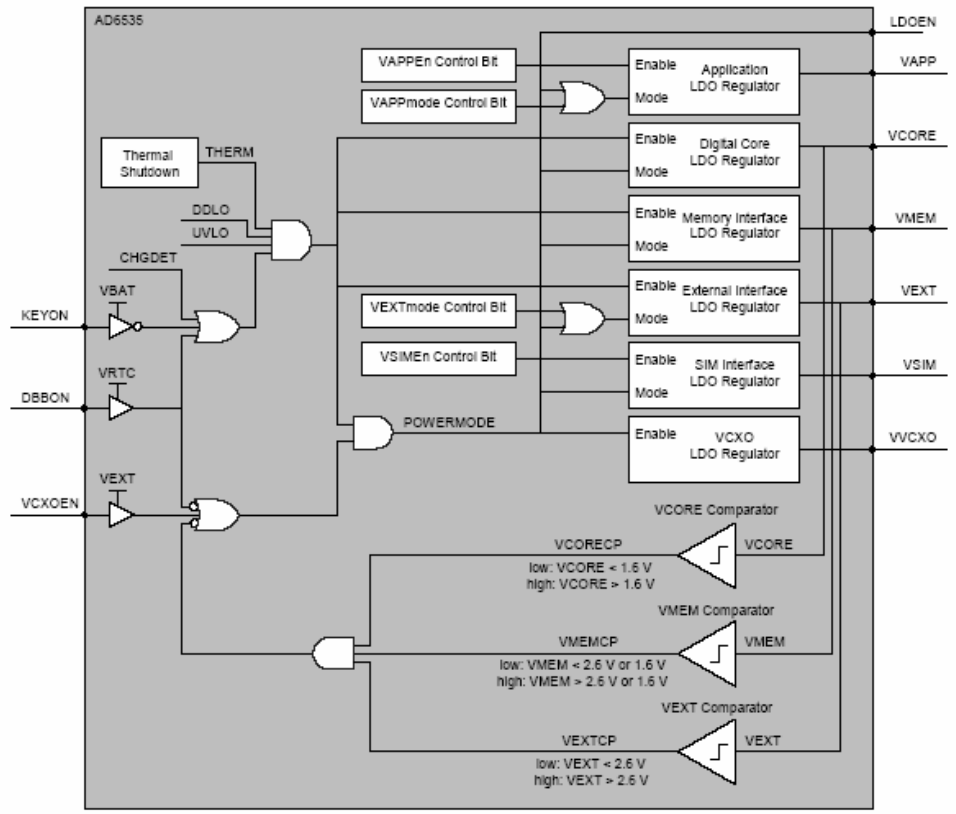


Figure 3-14. AD6535 POWER MODE LOGIC

2. LDO Block

1. There are 8 LDOs in the AD6535.
   - VCORE : supplies Digital baseband Processor core and AD6535 digital core
   - VMEM : supplies external memory and the interface to the external memory on the digital baseband processor (1,8V or 2.8V, 150mA)
   - VEXT : supplies Radio digital interface and high voltage interface (2.8V, 170mA)
   - VSIM : supplies the SIM interface circuitry on the digital processor and SIM card (2.85V, 20mA)
   - VRTC : supplies the Real-Time Clock module (1.8 V, 20 μA)
   - VABB : supplies the analog portions of the AD6537B
   - VMIC : supplies the microphone interface circuitry (2.5 V, 1 mA)
   - VVCXO : supplies the voltage controlled crystal oscillator (2.75 V, 10 mA)
   - VBACK : charges the backup battery and supplies the RTC regulator (2.8V, 1.8V)
   - VAPP : supplies application co-processors such as a touch screen digitizer (3.0V, 1.8V)
   - VUSB : supplies the USB interface.

3. Battery Charging Block

1. It can be used to charge Lithium Ion batteries. Charger initialization, trickle charging, and Li-Ion charging control are implemented in hardware.
2. Charging Process
   - Check charger is inserted or not
   - If AD6535 detects that Charger is inserted, the CC-CV charging starts.
   - Exception : When battery voltage is lower than 3.2V, the precharge(low current charge mode) starts firstly.
   - And the battery voltage reach to 3.2V the CC-CV charging starts.
3. Pins used for charging
   - VCHG : charger supply.
   - GATEDRIVE : charge DAC output
   - ISENSE : charge current sense input
   - VBATSENSE : battery voltage sense input.
   - BATTYPE : battery type identification input
   - REFCHG : voltage reference output
4. TA (Travel Adaptor)
   - Input voltage: AC 85V ~ 260V, 50~60Hz
   - Output voltage: DC 5.2V (0.2 V)
   - Output current: Max 800mA (50mA)
5. Battery
   - Li-ion battery (Max 4.2V, Nom 3.7V)
   - Standard battery: Capacity - 830mAh

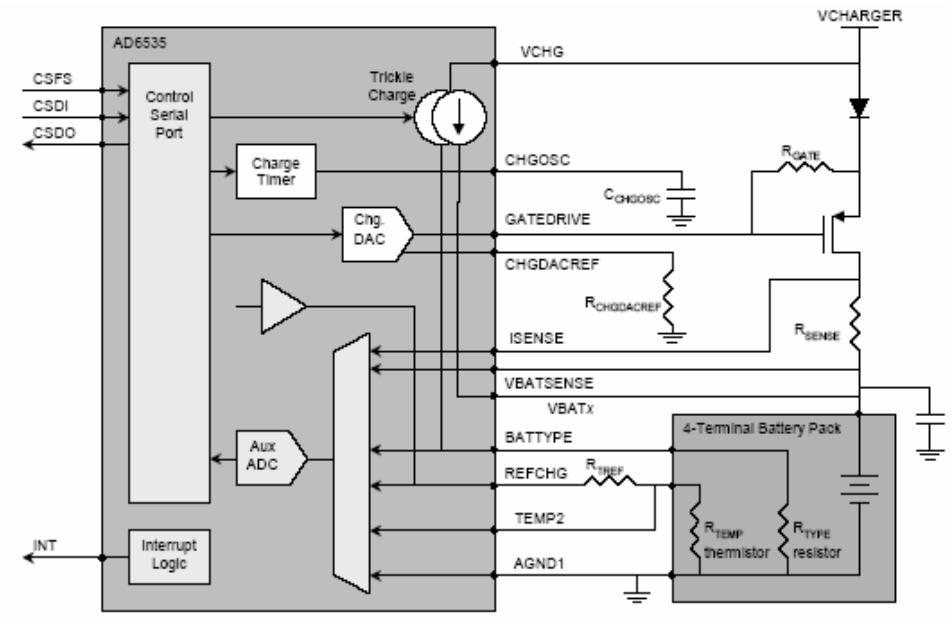


Figure 3-15. AD6535 BATTERY CHARGING BLOCK

3.6 Charging IC (ISL6299, U205)

Charging IC

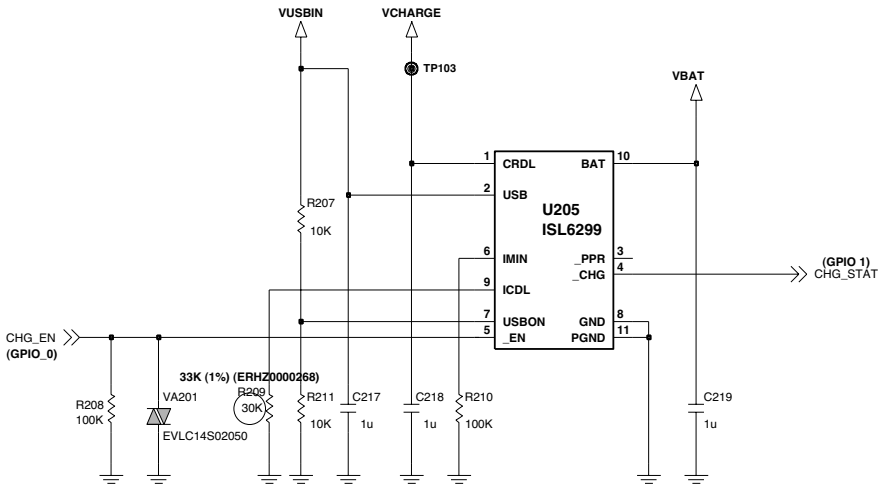


Figure 3-16. CIRCUIT FOR BATTERY CHARGING

The ISL6299 is designed for a single-cell Li-ion or Li-polymer battery charging circuit that accepts both a USB port and a desktop cradle as its power source.

Input Auto Selection

When both input sources are present, the charger selects only one power source to charge the battery. When the CRDL input is higher than the POR threshold, CRDL is selected as the power source. Otherwise the USB input is selected. If the CRDL input voltage is below the battery voltage but the USB input voltage is higher than the battery voltage, then the USB input is used to charge the battery. The control circuit always breaks both internal power devices before switching from one power source to the other to avoid a cross conduction of both power MOSFETs.

USB Charge Current

When the USB port is selected as the power source, the charge current enabled by the logic input at the USBON pin. When the USBON is driven to logic LOW, the charger is disabled. When the USBON is driven to logic HIGH, the charge current is fixed at a typical value of 380mA. Thus for the USB input, the USBON pin has a similar function as the EN pin. The following table describes the USB charge control by both the USBON pin and EN pin The USBON pin is equivalent to a logic LOW when left floating. Typically the P-channel MOSFET for the USB input has an rDS(ON) of 700mΩ at room temperature. With a 380mA charge current, the typical head room is 260mV. Thus, if the input voltage drops to a level that the voltage difference between the USB pin and the BAT pin is less than 260mV, the rDS(ON) becomes a limiting factor of the charge current; and the charger drops out the constant current regulation.

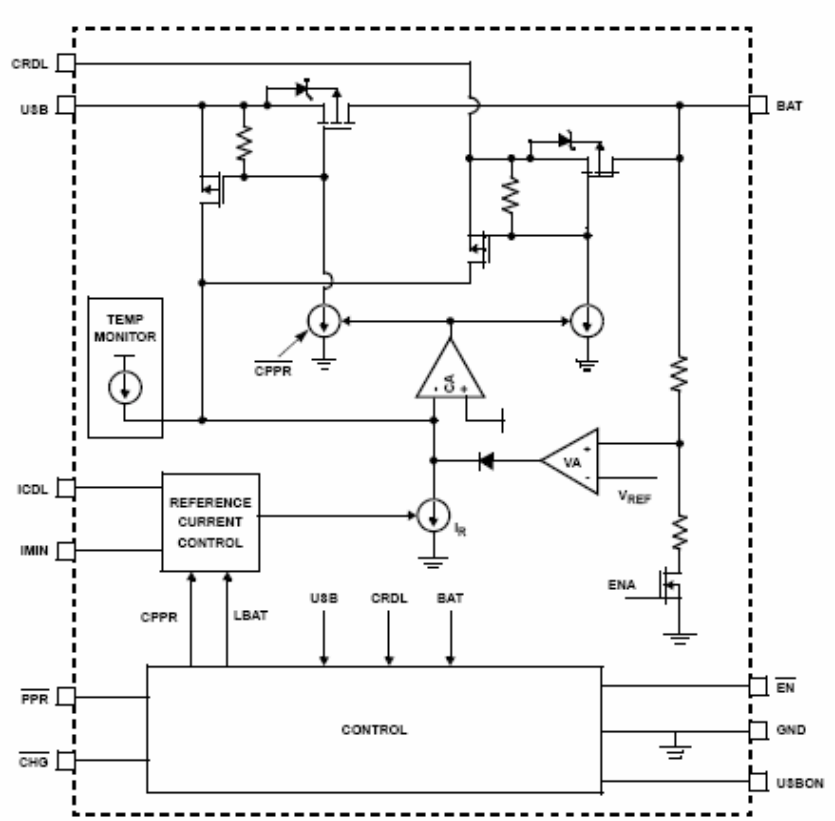


Figure 3-17. BLOCKDIAGRAM

Cradle Charge Current

The cradle charge current is enabled by the EN pin only, the USBON pin has no control on the cradle charge current. The cradle charge current is programmed with the external resistor connected between the ICDL pin and the GND pin. The current can be calculated with one of the equations given in the ICDL pin description. Two equations are used for the cradle current calculation, each corresponds to a different range of currents. The typical rDS(ON) of the P-channel MOSFET for the CRDL input is 600mΩ at room temperature. When the head room between the input and output voltages is small, the actual charge current, similar to the USB case, could be limited by the rDS(ON). On the other hand, if the head room between the input and output voltages is large, the charge current may be limited by the thermal foldback threshold.

Floating Charge Voltage

The floating voltage during the constant voltage phase is 4.2V. The floating voltage has an 1% accuracy over the ambient temperature range of -40˚C to 70˚C.

Trickle Charge Current

When the battery voltage is below the minimum battery voltage VMIN given in the electrical specification, the charger operates in a trickle/preconditioning mode, where the charge current is typically 14% of the programmed charge current for the cradle input. If power comes from the USB input, the trickle mode current is approximately 53mA.

End-of-Charge Indication

The CHG pin internal open-drain MOSFET turns off when the charge current falls below the IMIN threshold, which is programmable for the cradle input and fixed for the USB input. Once the end-of charge-current is reached, the CHG status will be latched. The latch can be reset at one of the following conditions:

1. The part is disabled and re-enabled
2. The selected input source has been removed and reapplied
3. The USBON turns LOW and turns back to HIGH for the USB input
4. The BAT pin voltage falls below the CV mode threshold

Regardless of the CHG pin status, however, the charger does not turn off as long as an input power source is attached.

Power Presence Indication

When either the USB or the cradle input voltage is above the POR threshold, the PPR pin internal open-drain MOSFET turns on indicating the presence of input power.

Power-Good Range

Even if there is a power present, the charger will not deliver any current to the output if the powergood conditions are not met. The following two conditions together define the power-good voltage range:

1. VCDRL or VUSB > VPOR
2. VCDRL or VUSB - VBAT > VOS

where the VOS is the offset voltage for the input and output voltage comparator, discussed shortly.
Both VPOR, VOS have hysteresis, as given in the Electrical Specification table.
The charger will not charge the battery if the input voltage does not meet the power-good conditions.

Thermal Foldback (Thermaguard™)

The thermal foldback function reduces the charge current when the internal temperature reaches the thermal foldback threshold, which is typically 100°C. This protects the charger
from excessive thermal stress at high input voltages.

3.7 CAMERA IC(AIT811T,U103)

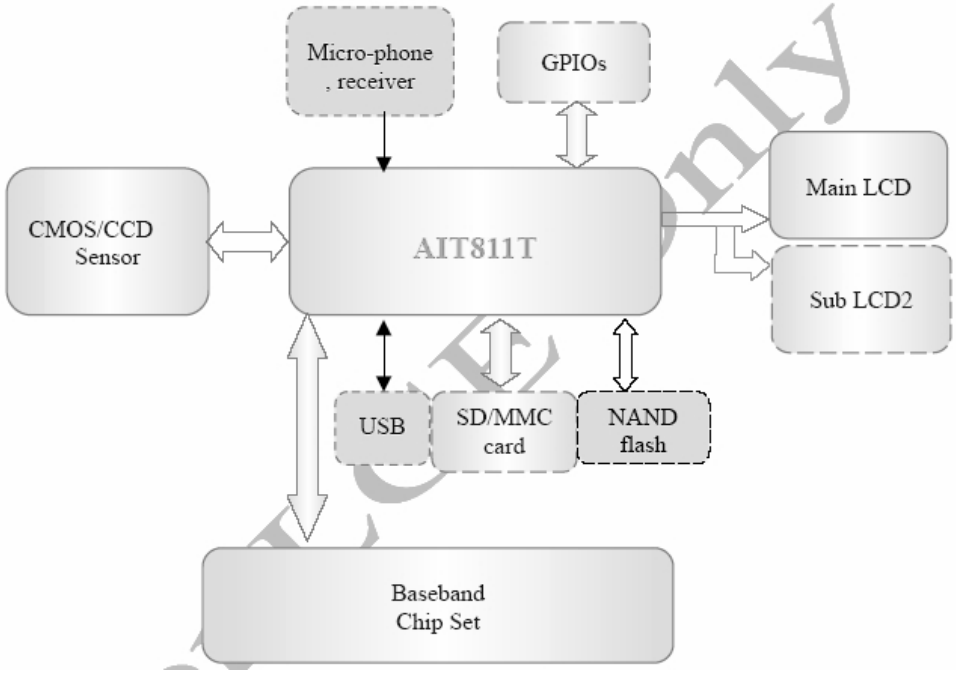


Figure 3-18. AIT811T APPLICATION BLOCKDIAGRAM

Multimedia & Camera

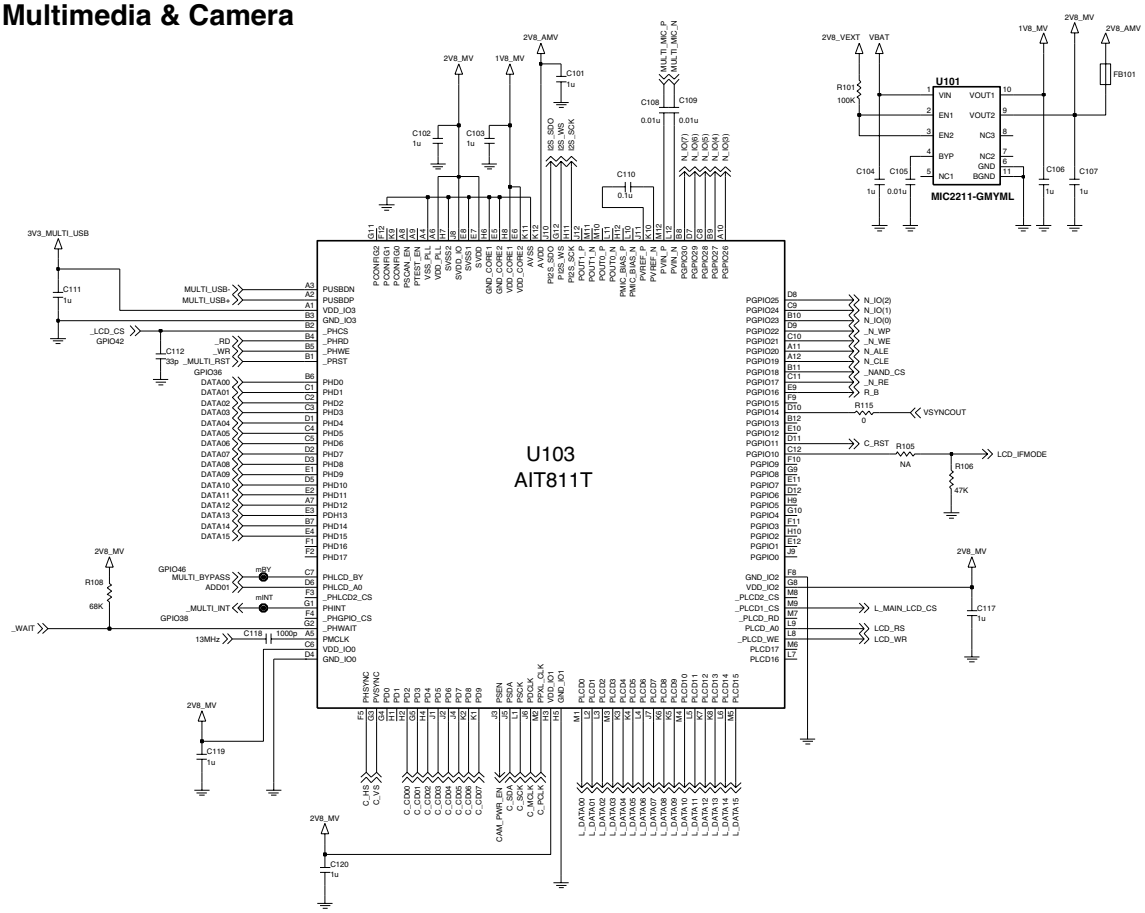


Figure 3-19. AIT811T CIRCUIT

3.8 MIDI IC(YMU787,U202)

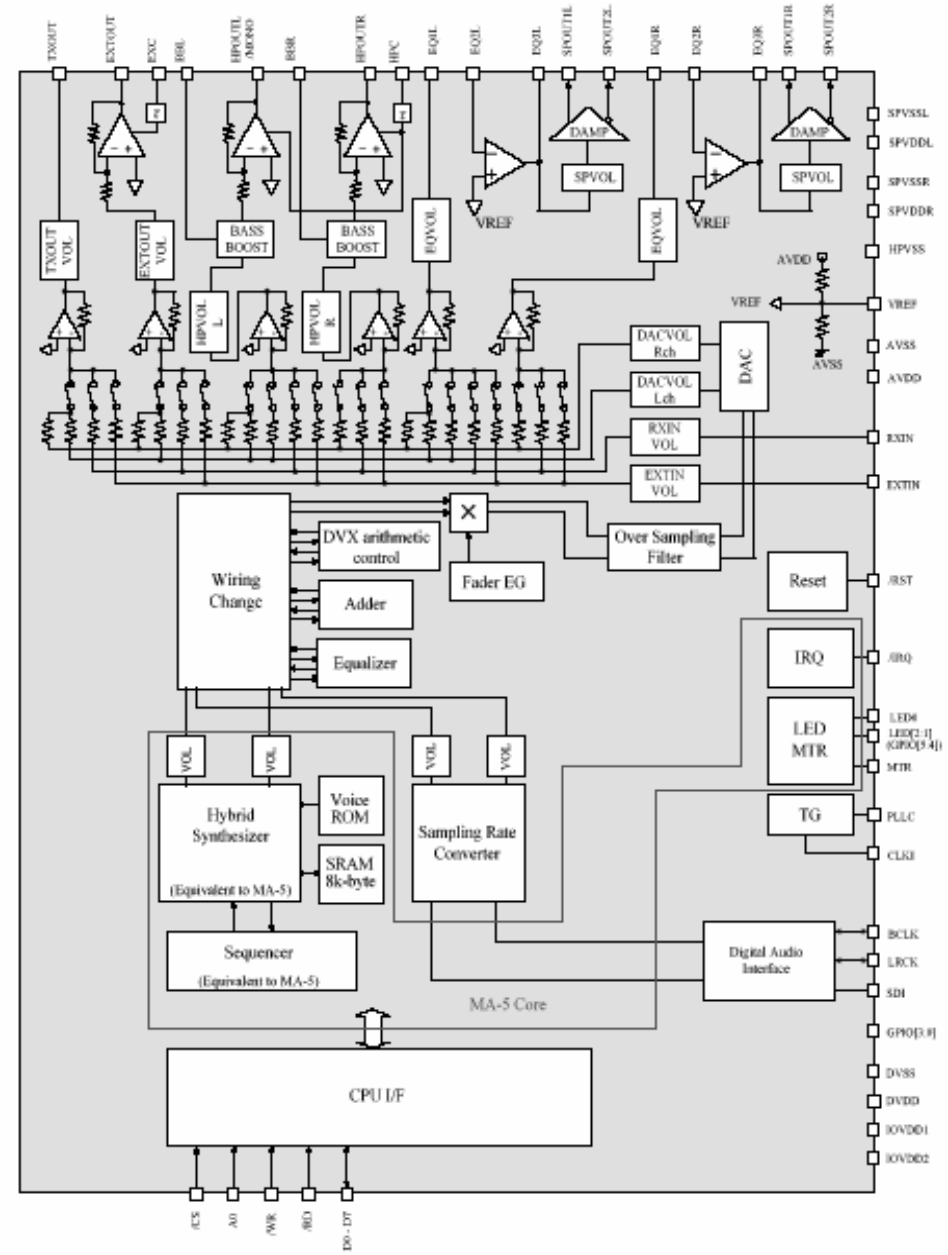


Figure 3-20. YMU787 BLOCKDIAGRAM

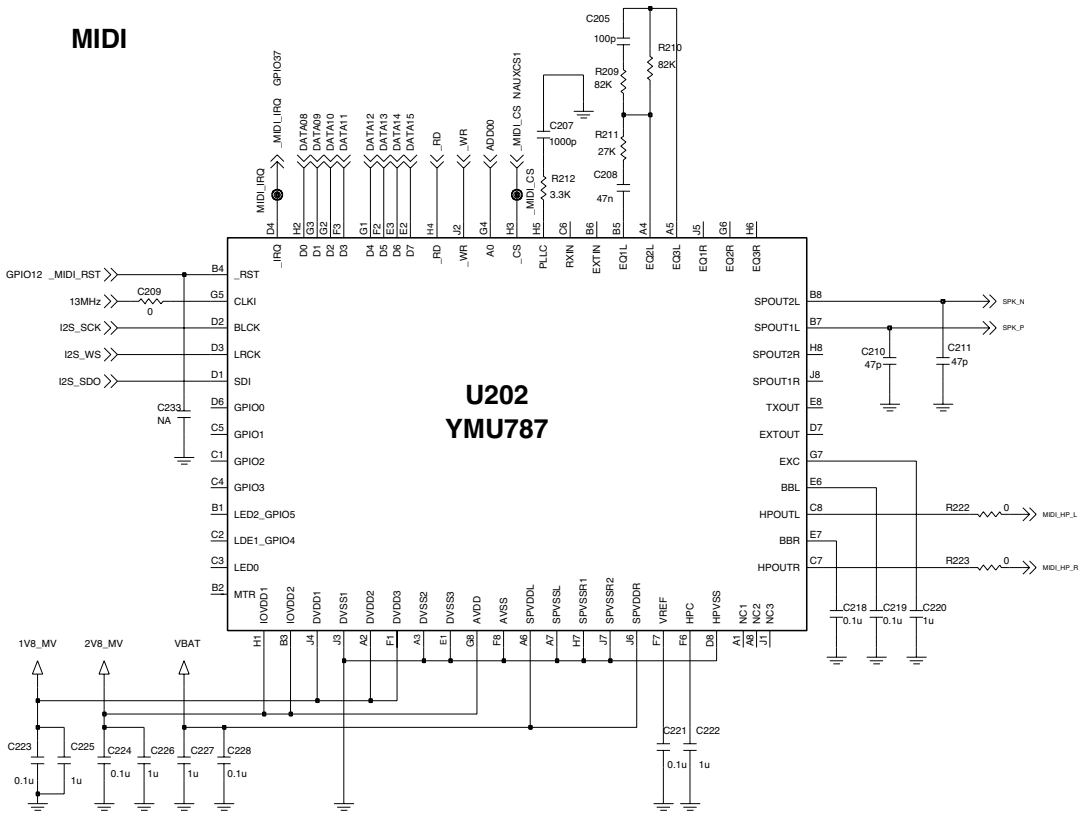


Figure 3-21. YMU787 CIRCUIT DIAGRAM

CPU INTERFACE

CPU interface is an 8-bit parallel.

4 control signal(/wr,/rd,/cs,A0 pin), 8 data bit(D0 to D7), and 1 interrupt pin(/IRQ), totaling 13 pins are connected to the external CPU. This block controls the writing and reading of data by the input polarity of control signal

INTERFACE REGISTER

This registeris able to access directly ffrom the external CPU. There are 2 bytes spaces. The Intermediate register can be accessed through the interface register.

INTERMEDIATE REGISTER

This register is accessed through the Interface register.

It is composed to access a latter control register and ROM/SRAM through Intermediate register. This register is called “Intermediate register” since this exists in the middle of the interface register and the Control register. In the Intermediate register, there are some registers to control various functions.

3. TECHNICAL BRIEF

CONTROL REGISTER;ROM/SRAM

The Control register and ROM/SRAM are accessed from"Instantaneous write register","Delayed write register", and "Instantaneous read register"in the intermediate register.

In the control register, there is a register to control the following synthesizer mainly. The voice parameter for FM(GM 128 voices+DRUM 40 voices)and wave data for WT are stored in ROM. SRAM is used at the download of arbitary FM voice parameter and Wave data for WT. moreover, it is used as storing buffer at the stream playback of PCM/ADPCM.

FIFO

This is an abbreviation of "First Input First Output" means the memory from which data is read in order of data written. There are 2 paths to write into FIFO in the Intermediate register.The"instantaneous write path" is for accessing the control register and ROM/SRAM immediately,also "Delayed write path"is for accessing the control register after managing time through the sequencer.FIFO size of Instantaneous path is 64 byte, and its size of Delayed path is 512-byte.

SEQUENCER

This is for interpreting the contents of data which is written into the "Delayed write path" Generally, "Music data" is written into the Delayed write path. It interprets the contents of music data and controls the synthesizer after sequencer, and then plays the music.

Hybrid synthesizer

This device contains a built in polyphonic synthesizer that adopts a stereophonic hybrid system that generate up to 64tones.

FM synthesizer, WT synthesizer, stream playback, HV synthesizer, and AL synthesizer are available.

DIGITAL AUDIO INPUT INTERFACE

This is a three wires type serial interface.The data length is 16bits.

DPLL SECTION/SAMPLING RATE CONVERTER SECTION

Sampling frequencies of signals from the digital audio interface section are changed into 48Khz.

DIGITAL EQUALIZER SECTION

This is a digital equalizer. Voice of signals from the Hybrid Synthesizer section and voice of digital audio signals are adjusted.

DVX ARITHMETIC CONTROL

Two-channel virtual speaker image function that is based on DVX technology makes it possible to create natural stereo sound under the two closely spaced speakers.

OVER SAMPLING FILTER

4 Times of over sampling filter. It converts a signal of sampling frequency 48Khz into a signal of 192Khz,and then send to DAC

GENERAL PARALLEL I/O PORT SECTION(GPIO)

There are six general parallel I/O ports. It is possible to read and write from the Intermediate register.

LED,VIBRATOR CONTROL

It is possible to synchronize an LED and vibrator with a play, and to control. Asynchronous control With a play is also supported. It supports 3 color LED control and it is possible to display 7 colors In maximum.

CLOCK GENERATING BLOCK

This device supports a clock input ranging from 1.5Mhz to 27Mhz.
It is a block to generate a clock which is needed inside of LSI in the PLL.

DAC

It converts digital signals from a synthesizer and a digital audio section into analog signals.
Its resolution is 16bits.

ANALOG LINE INPUT SECTION(EXTIN,RXIN)

External audio signal and receiver audio signal are inputted.
There is a Volume to adjust the level in each.

MIXER SECTION

Selection of an input source(DAC output, RXIN, and EXTIN) against each analog output(SPOUT, HPOUT,EXTOUT,TXOUT) and mixing are performed.

EQ AMPLIFIER SECTION

The change of filter characteristic and gain is possible by adjusting the resistors and external parts.

SPEAKER AMPLIFIER SECTION

The two digital speakers amplifier, which has a maximum output power of 500mW at SPVDDL/R=3.6V and RL=8ohm, is integrated in this device. There is a volume to adjust output level in the first stage of amplifier.

HEADPHONE AMPLIFIER SECTION(HPOUT)

This is an amplifier for stereophonic headphone(RL=16ohm)output.
When it is used as a monaural output, Rch becomes power-down.
In the previous part of it, there are a volume and a bass-boost circuit.

EXTERNAL OUTPUT AMPLIFIER SECTION(EXTOUT)

This is an amplifier for external output(RL=600ohm)
In the previous part of it, there is a volume to adjust the output level

ANALOG LINE OUTPUT SECTION(TXOUT)

This is monaural line output(RL=10kohm)
There is a volume to adjust the output level.

3.9 Keypad Switches and Scanning

KEY PCB CONN

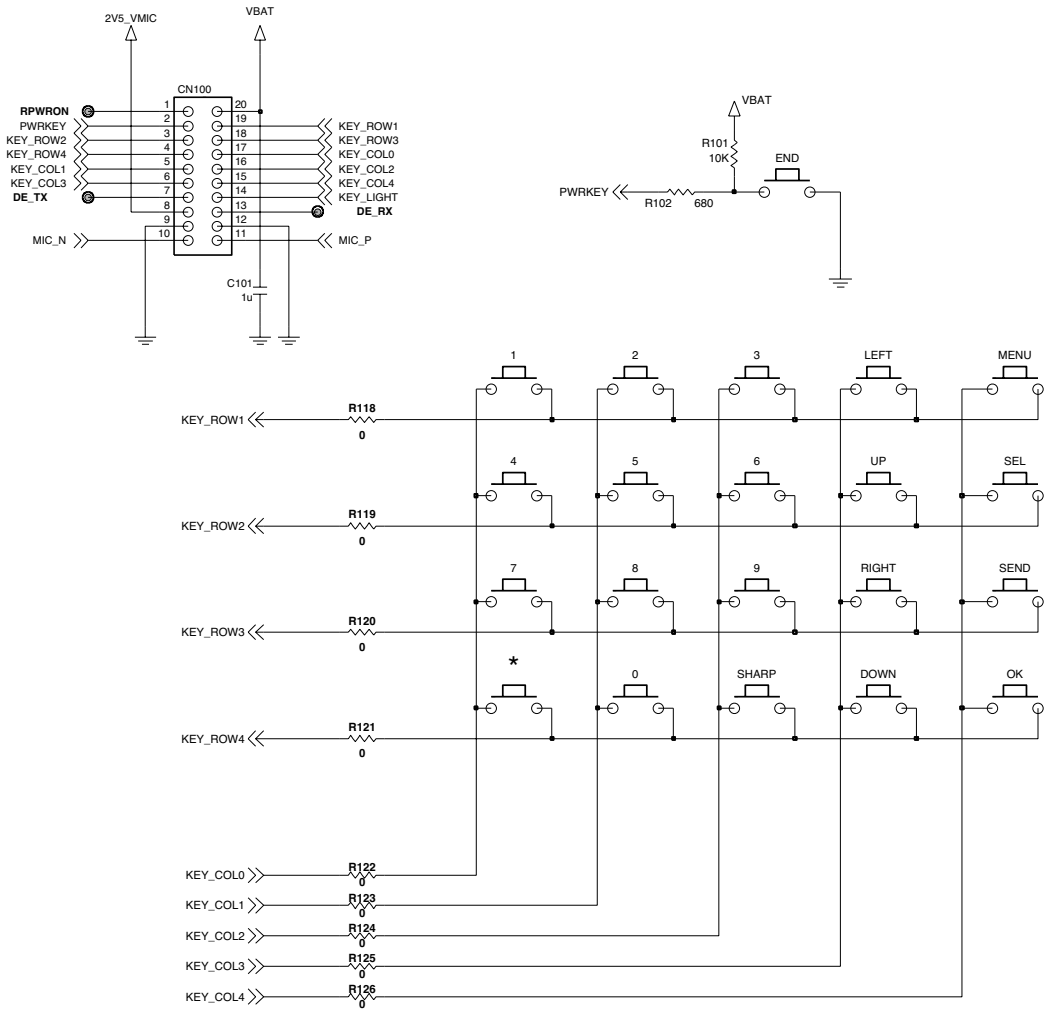


Figure 3-22. KEYPAD SWITCHES AND SCANNING

3.10 Microphone

The microphone is placed to the front cover and contacted to main PCB. The audio signal is passed to AIN1P and AININ pins of AD6535. The voltage supply VMIC is output from AD6535, and is a biased voltage for the AIN1P. The AIN1P and AIN1N signals are then A/D converted by the voiceband ADC part of AD6535.The digitized speech (PCM 8KHz ,16KHz) is then passed to the DSP section of AD6527B for processing (coding, interleaving etc).

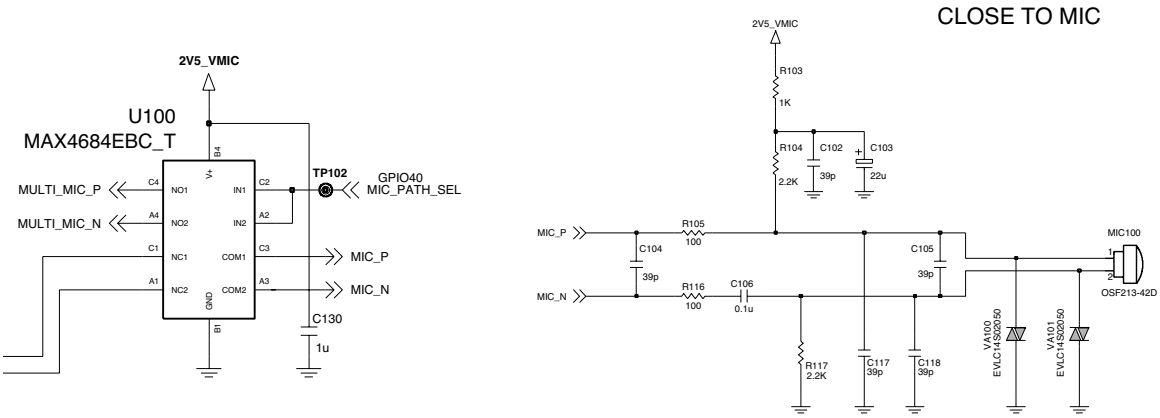


Figure 3-23. Connection between Microphone and AD6535

3.11 Main Speaker

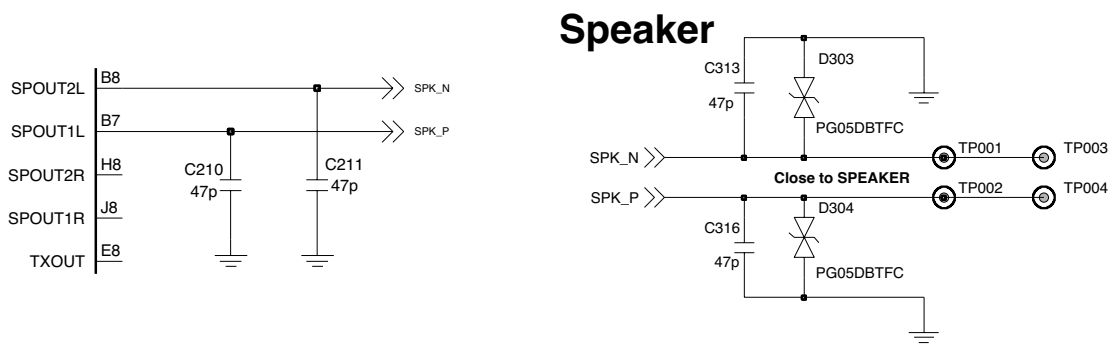


Figure 3-24. MAIN SPEAKER

3.12 Headset Interface

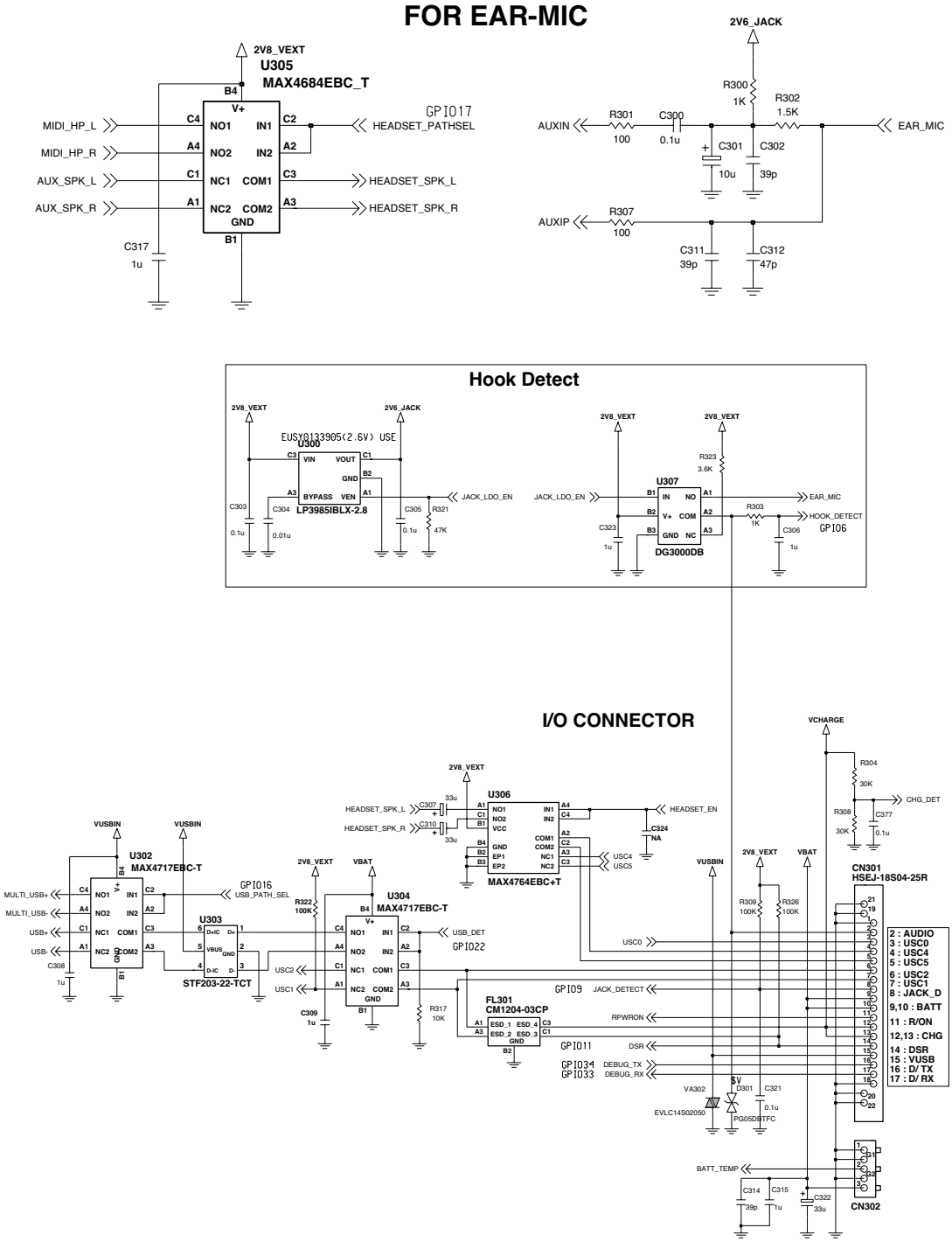


Figure 3-25. HEADSET JACK INTERFACE, HEADSET JACK ANALOG SWITCH

3.13 MEMORY(TOSHIBA, U204)

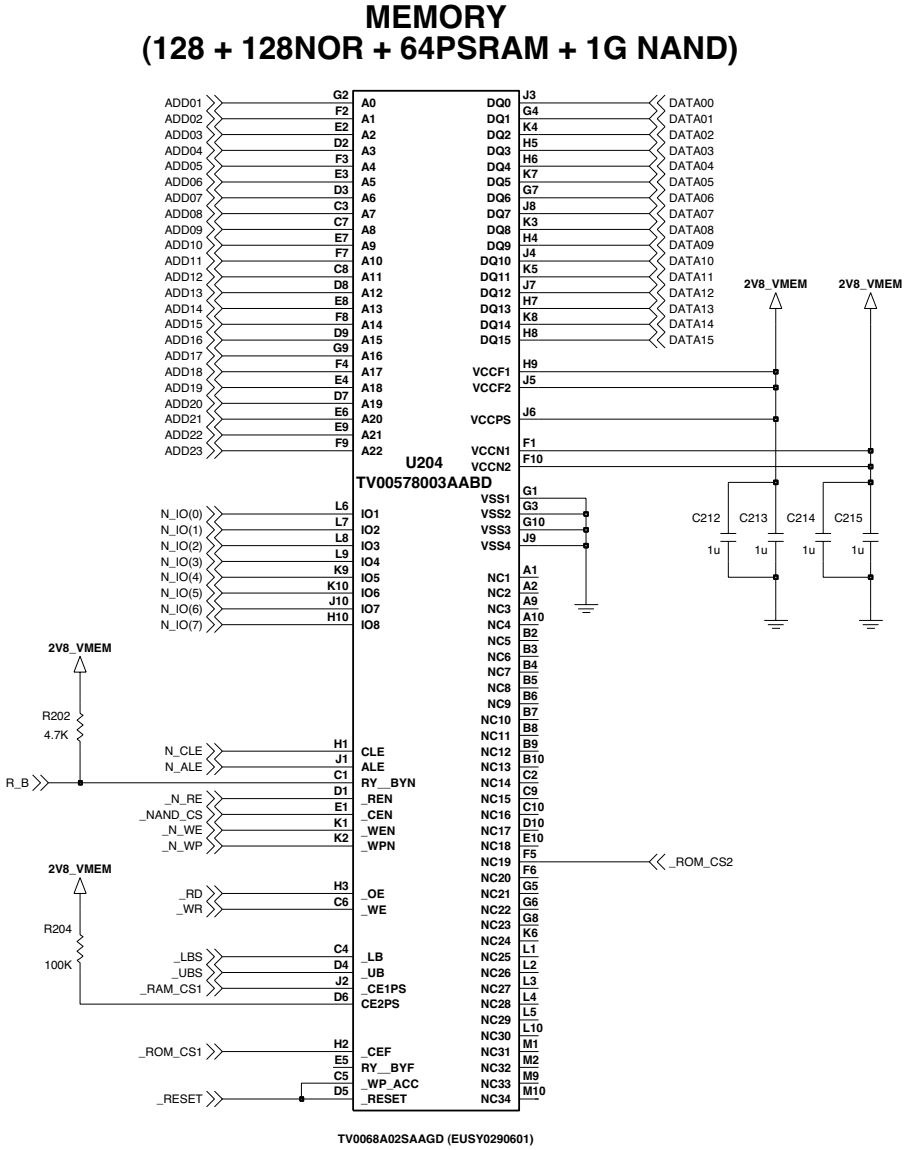


Figure 3-26. MEMORY

3.14 BLUETOOTH(LBMA-2C67B2,U202)

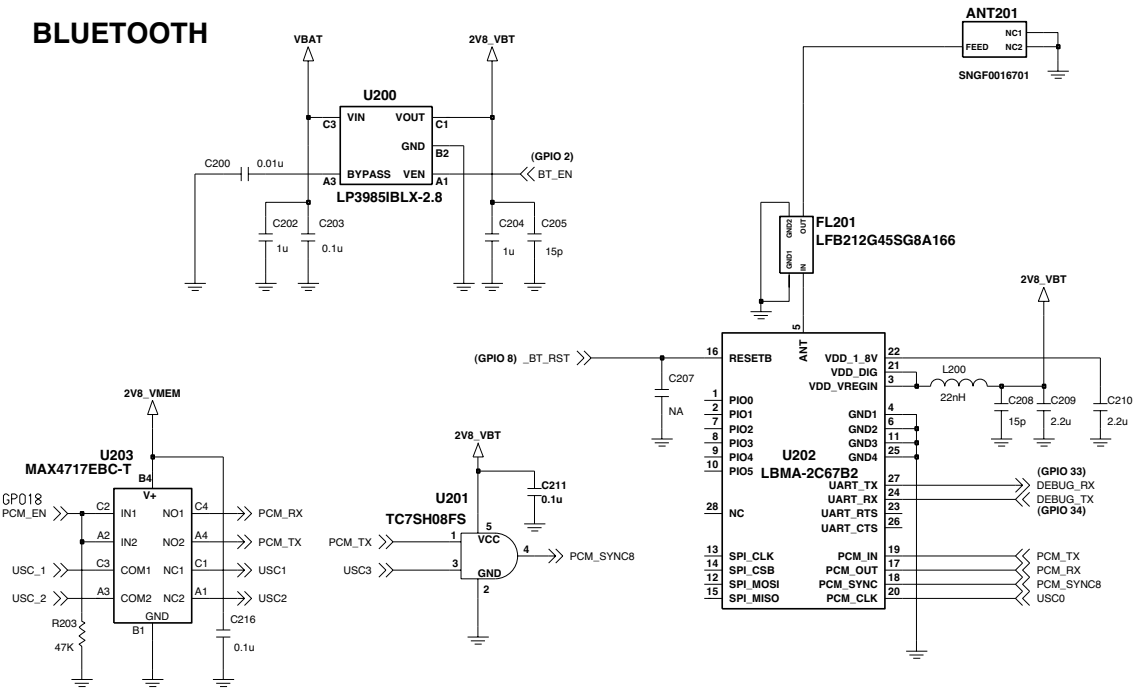


Figure 3-27. BT MODULE

3.15 CAMERA CONNECTOR, CAMERA LDO(CN202,U201)

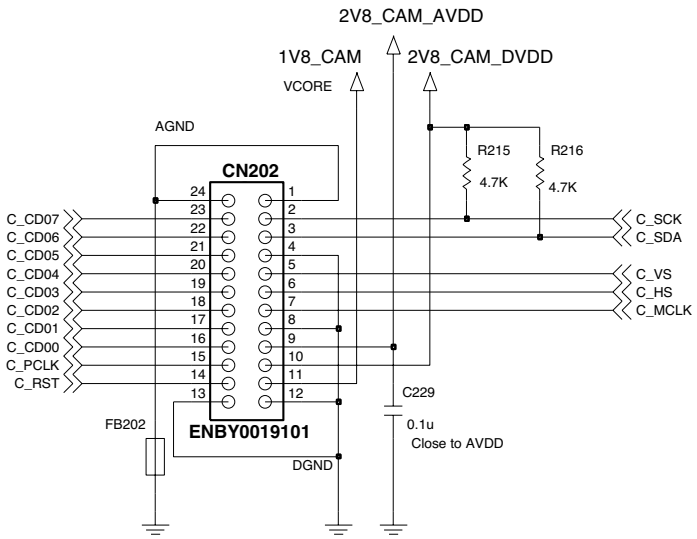


Figure 3-28. CAMERA CONNECTOR

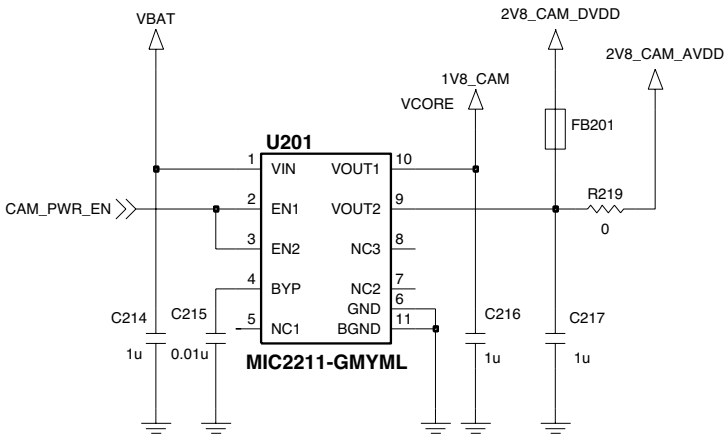


Figure 3-29. CAMERA LDO

3.16 KEY BACKLIGHT

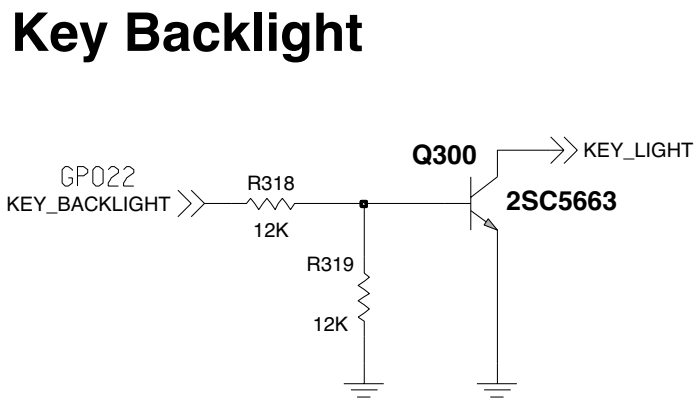


Figure 3-30. MAIN KEY BACKLIGHT

3.17 WHITE/FLASH LED LDO

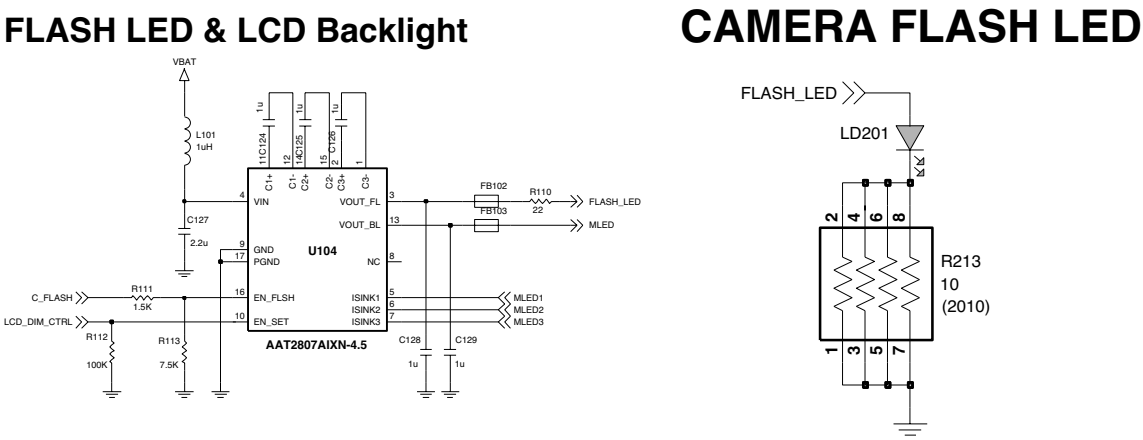


Figure 3-32. WHITE/FLASH LED LDO

3.18 FLIP SWITCH (U105)

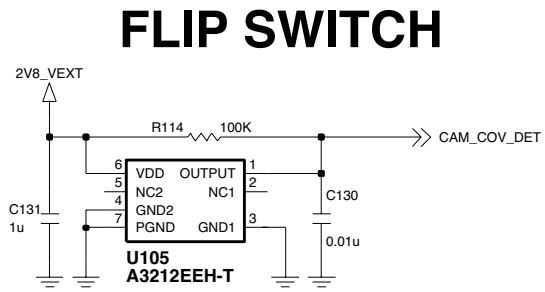


Figure 3-34. FLIP SWITCH

3.19 VIBRATOR

The vibrator is placed in main board. The vibrator is driven from VIBRATOR from AD6527B.

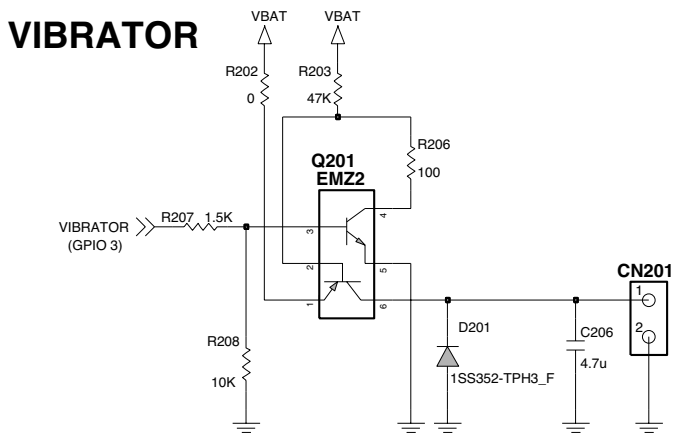


Figure 3-35. MOTOR

4. TROUBLE SHOOTING

4.1 RX Trouble

TEST POINT

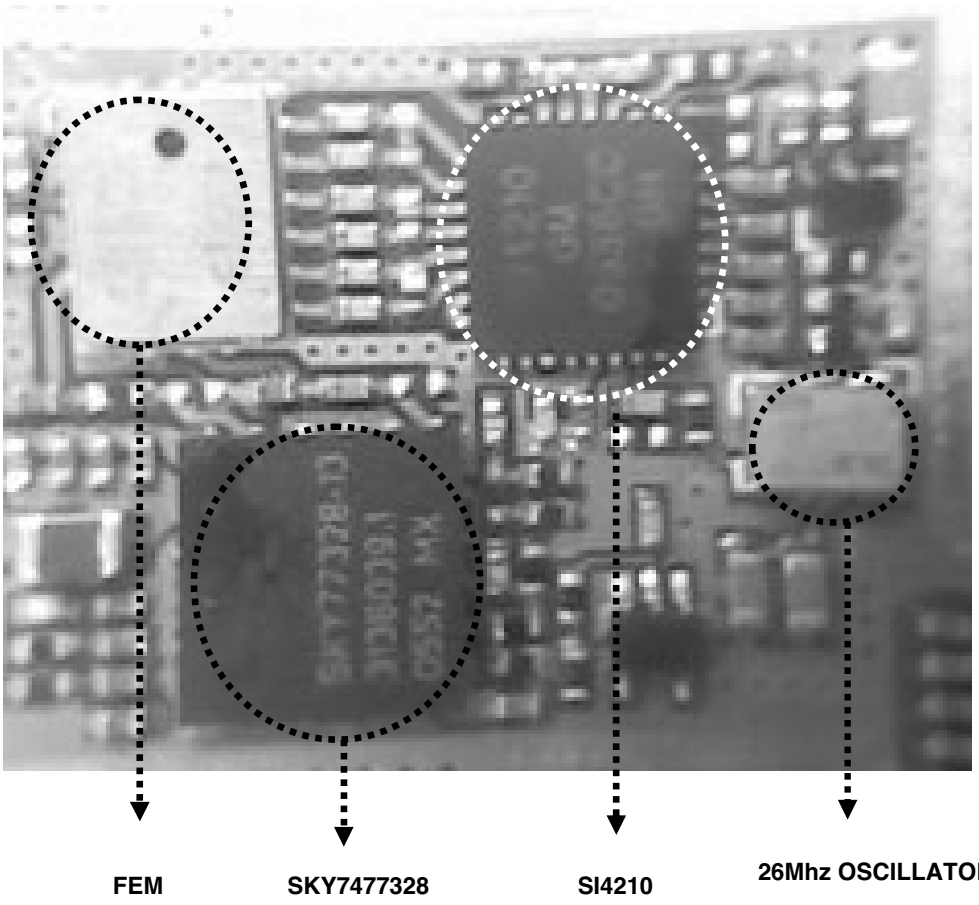
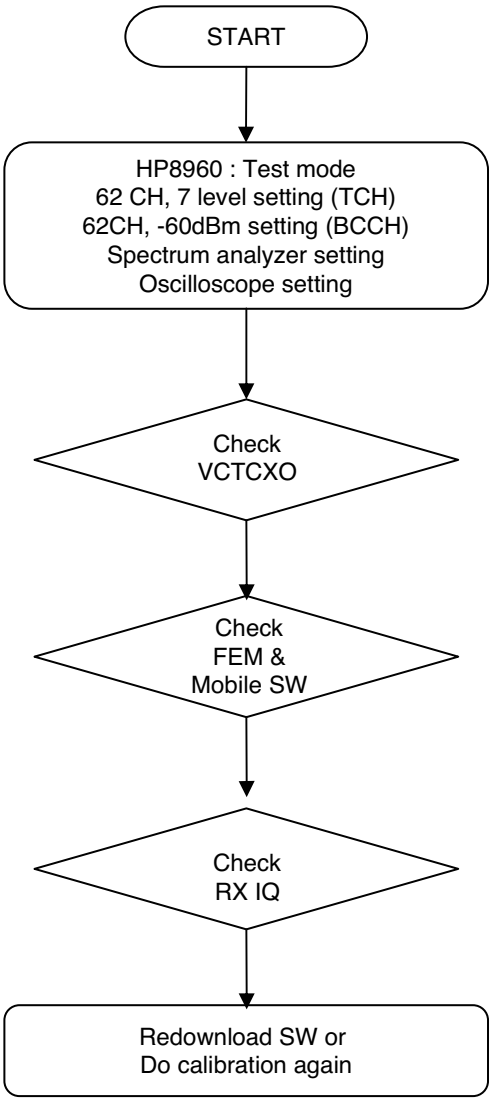


Figure 4-1

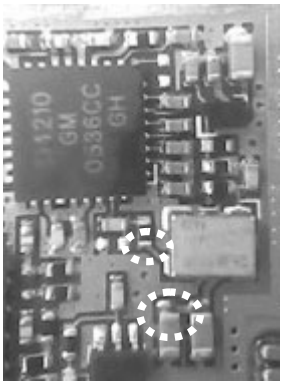
Checking Flow



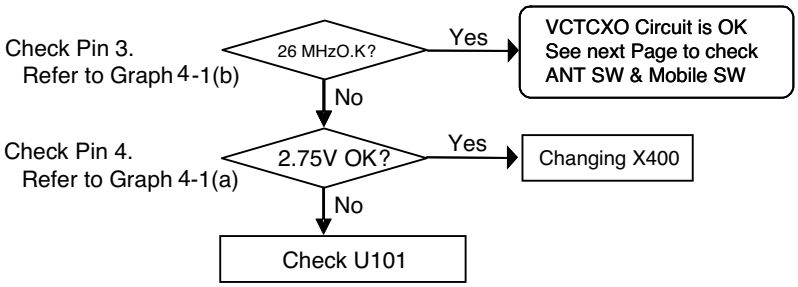
4. TROUBLE SHOOTING

(1) Checking VCTCXO Circuit

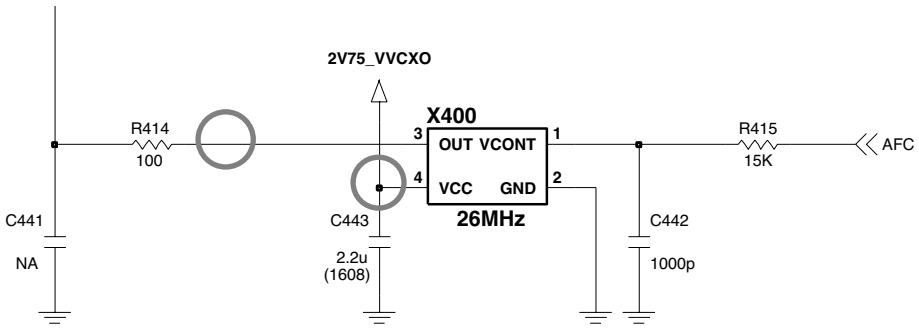
TEST POINT



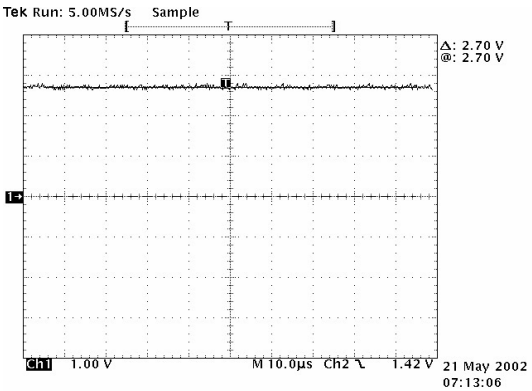
Checking Flow



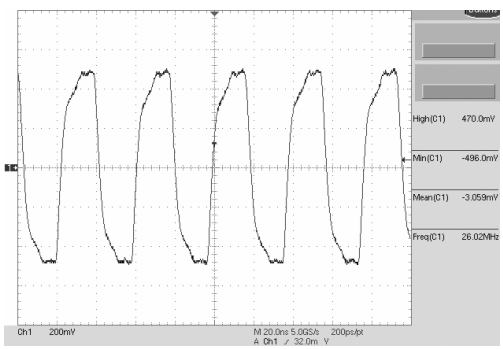
CIRCUIT



Waveform



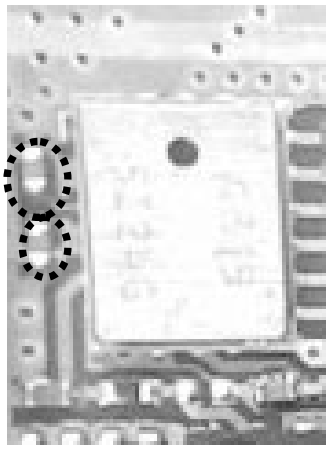
Graph 4-1(a)



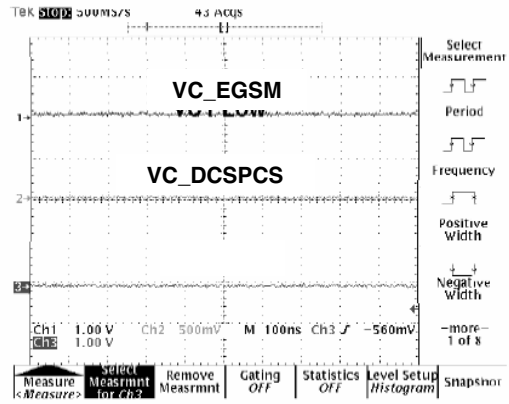
Graph 4-1(b)

(2) Checking FEM & Mobile SW

TEST POINT

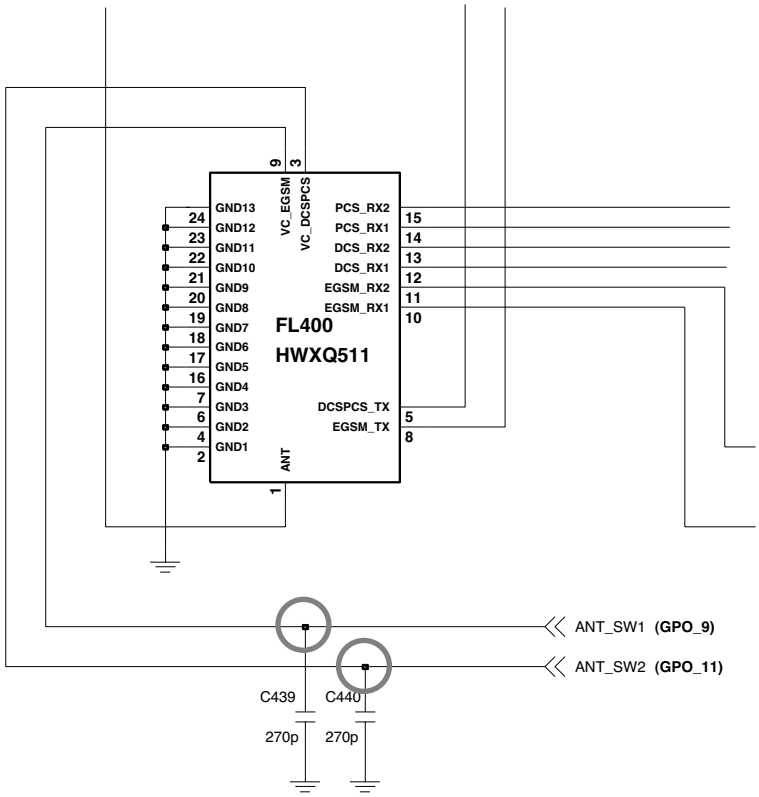


Waveform

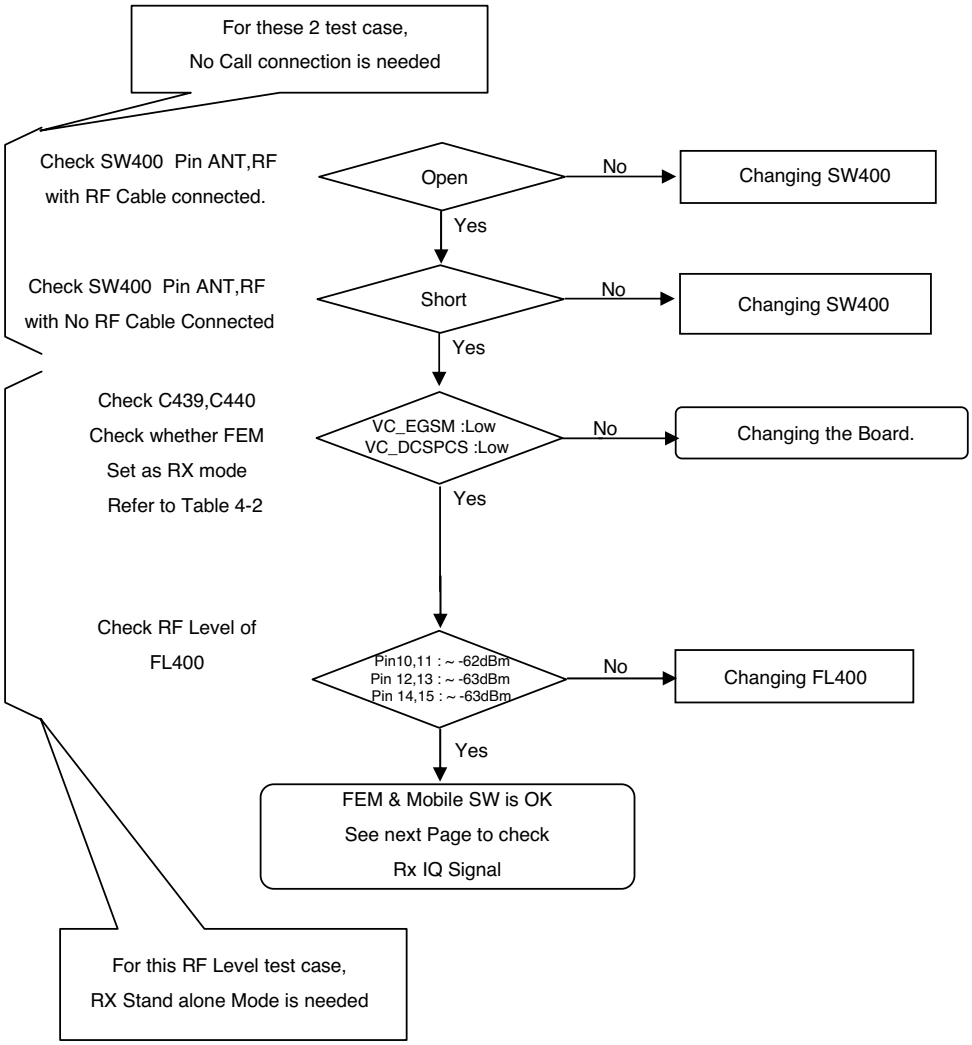


FEM Control GSM & DCS & EGSM
Graph 4-2(a)

CIRCUIT



Checking Flow

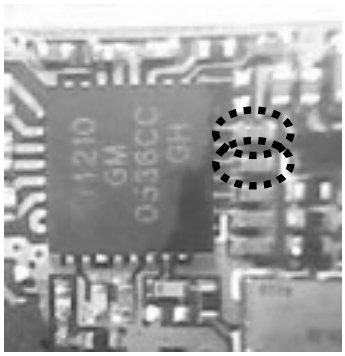


Select Mode	Vc(EGSM)	Vc(DCS/PCS)
EGSM-Rx	Low	Low
EGSM-Tx	High	Low
DCS-Rx	Low	Low
PCS-Rx	Low	Low
DCS/PCS-Tx	Low	High

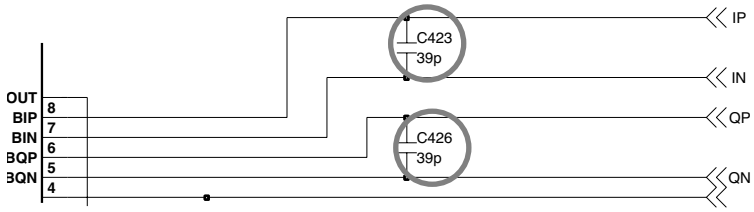
Table 4-2

(4) Checking RX IQ

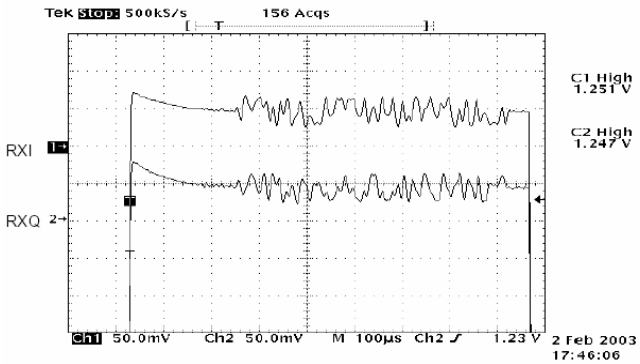
TEST POINT



CIRCUIT

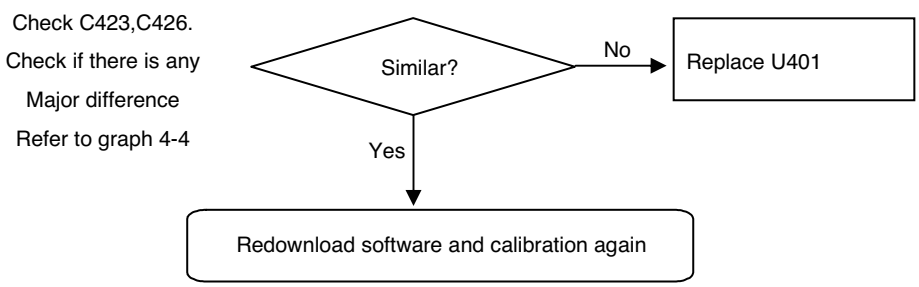


Waveform



Graph 4-4

Checking Flow



4.2 TX Trouble

TEST POINT

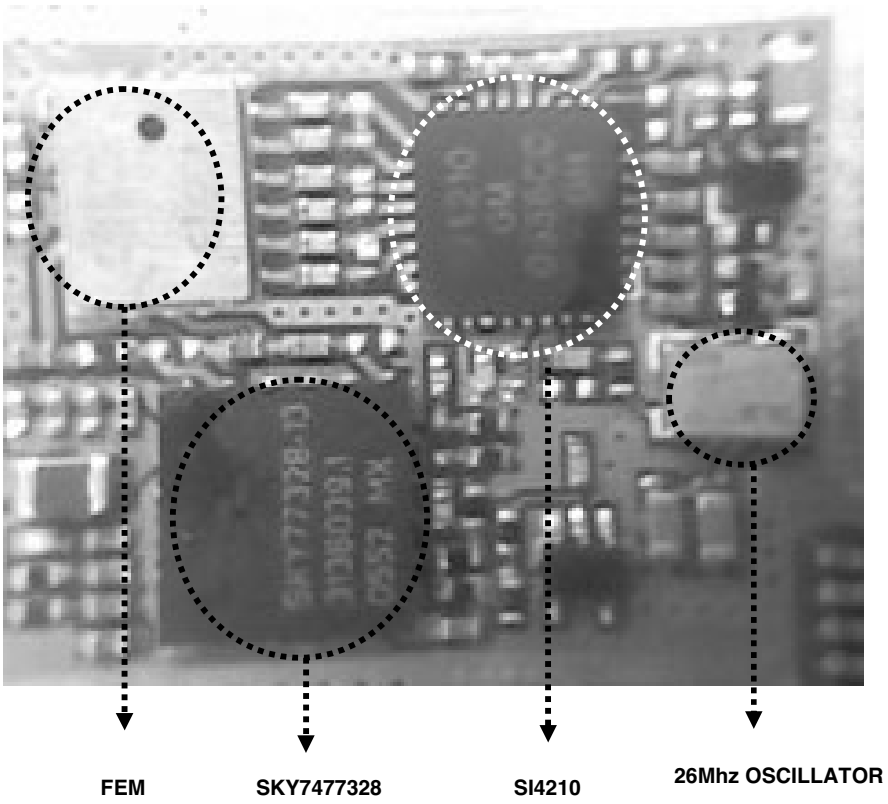
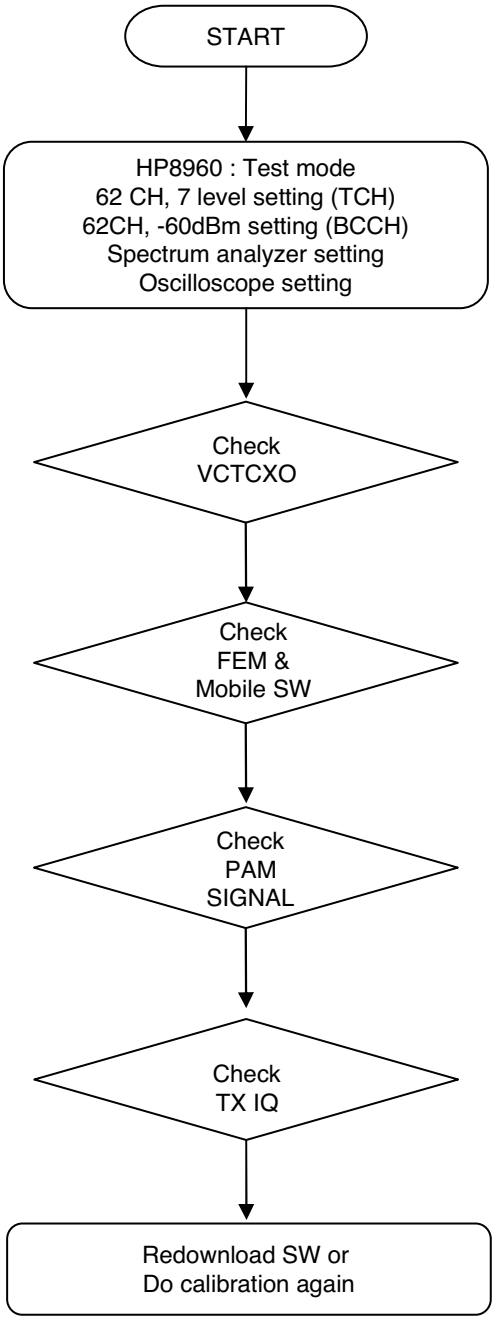


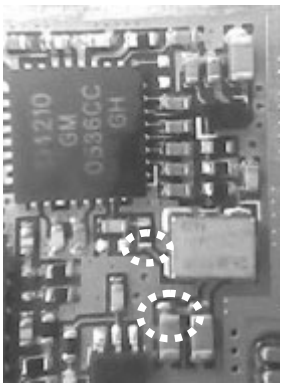
Figure 4-2

Checking Flow

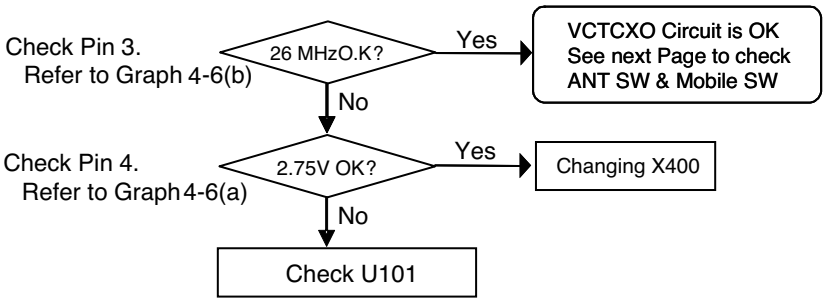


(1) Checking VCTCXO Circuit

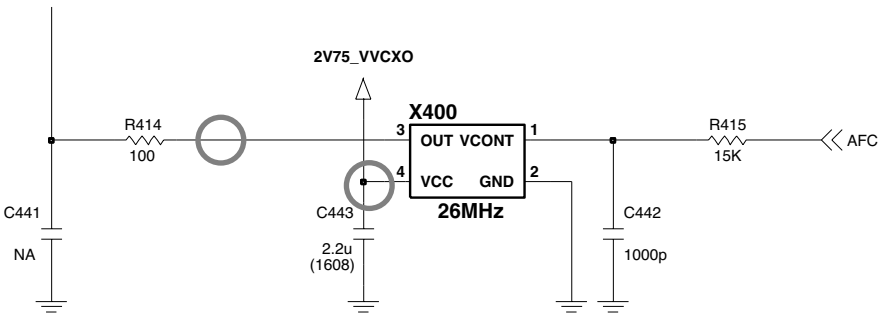
TEST POINT



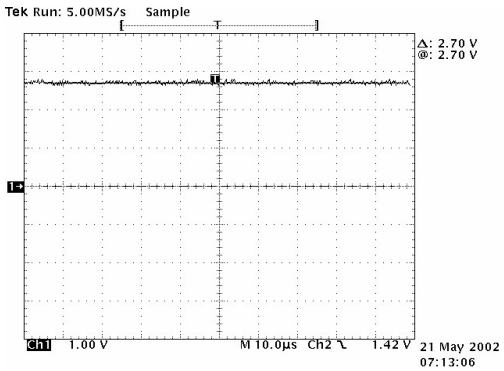
Checking Flow



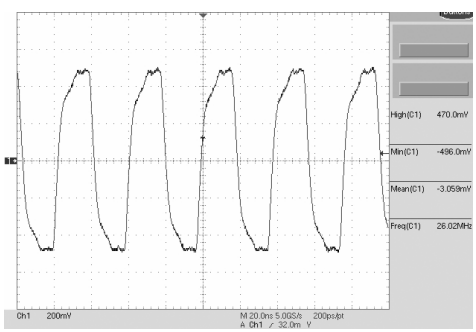
CIRCUIT



Waveform



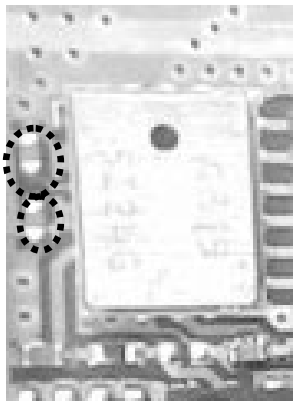
Graph 4-6(a)



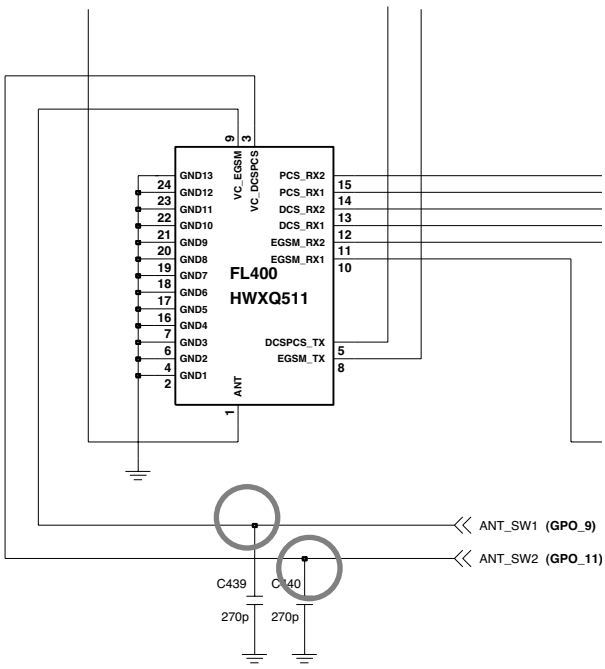
Graph 4-6(b)

(3) Checking Ant SW & Mobile SW

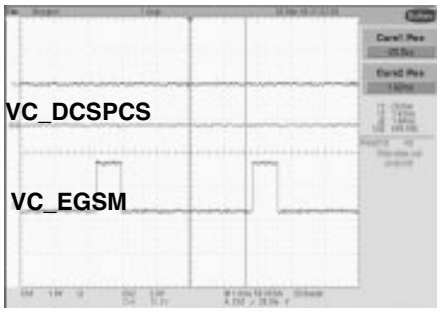
TEST POINT



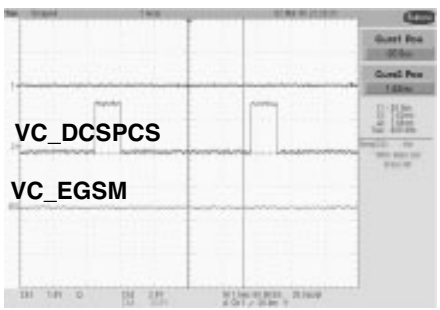
CIRCUIT



Waveform

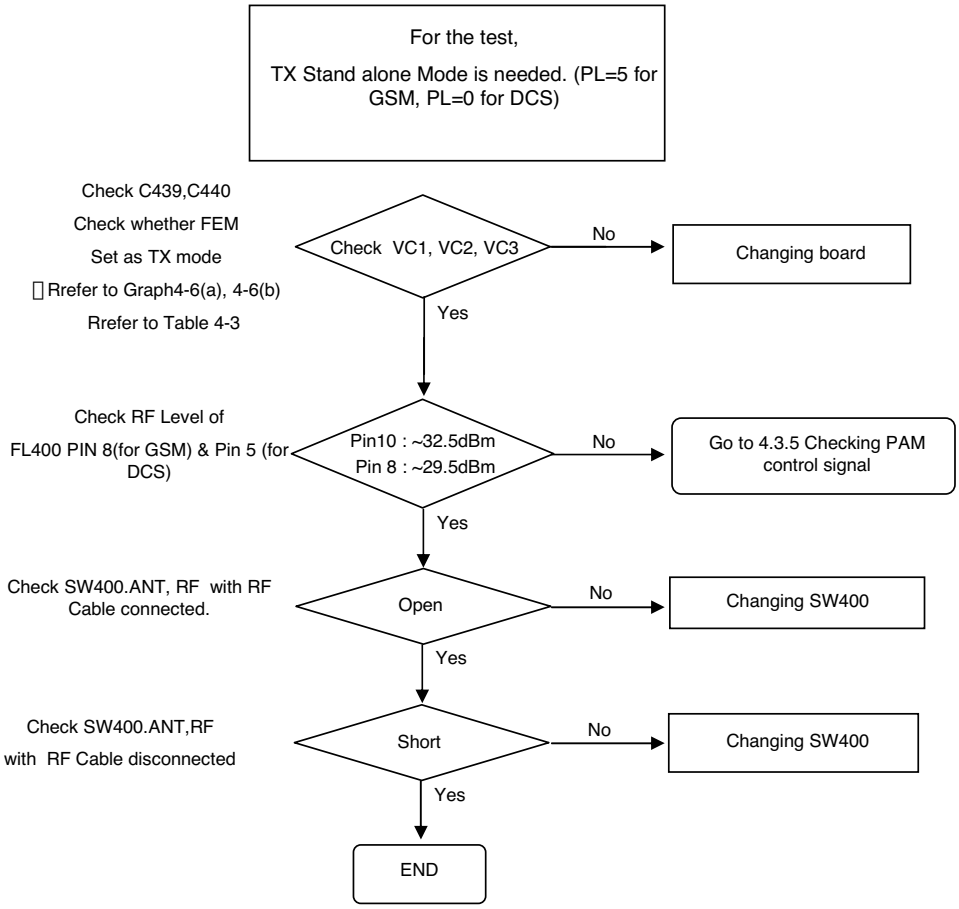


FEM Control EGSM
Graph 4-7(a)



FEM Control DCS & PCS
Graph 4-7(b)

Checking Flow

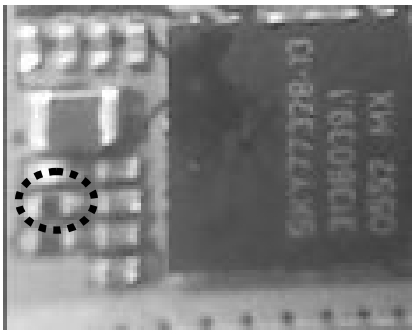


Select Mode	Vc(EGSM)	Vc(DCS/PCS)
EGSM-Rx	Low	Low
EGSM-Tx	High	Low
DCS-Rx	Low	Low
PCS-Rx	Low	Low
DCS/PCS-Tx	Low	High

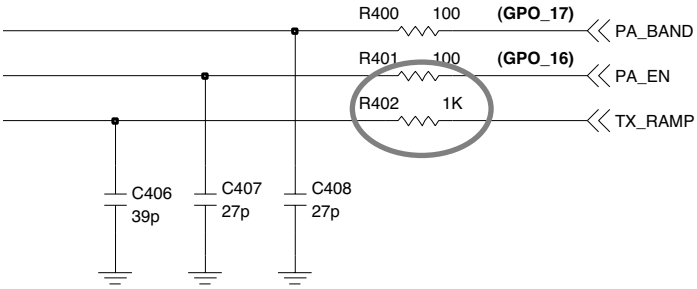
Table 4-2

(4) Checking PAM Control Signal

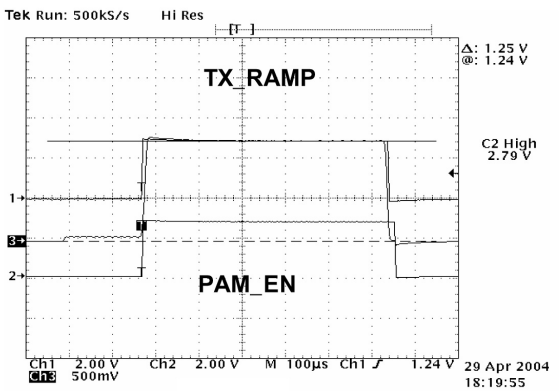
TEST POINT



CIRCUIT



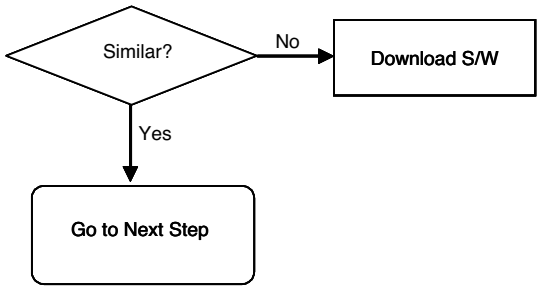
Waveform



Graph 4-8

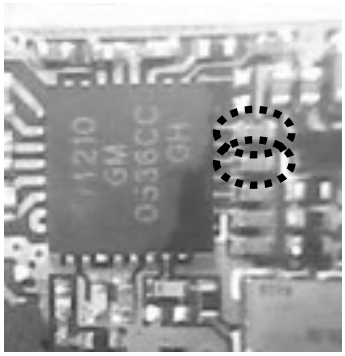
Checking Flow

Check TX_RAMP and PA_EN
Check if there is
Any Major Difference or not
Refer to Graph 4 - 8

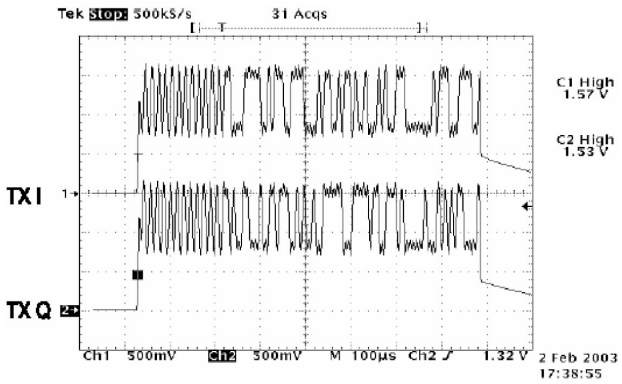


(5) Checking TX IQ

TEST POINT

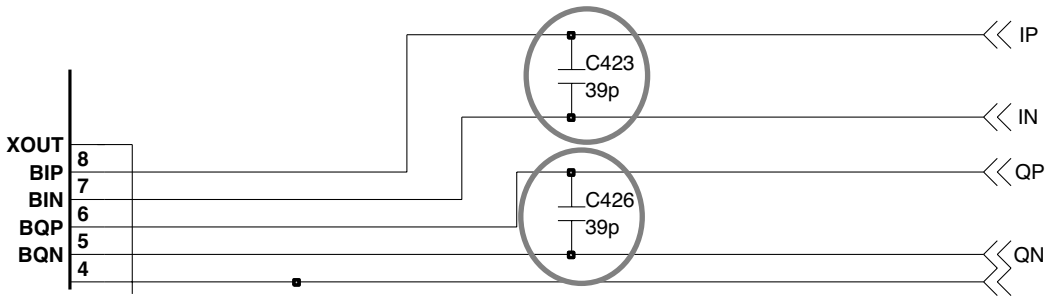


Waveform

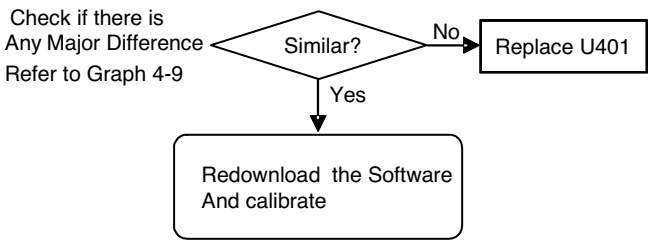


Graph 4-9

CIRCUIT



Checking Flow



4.3 Power On Trouble

TEST POINT

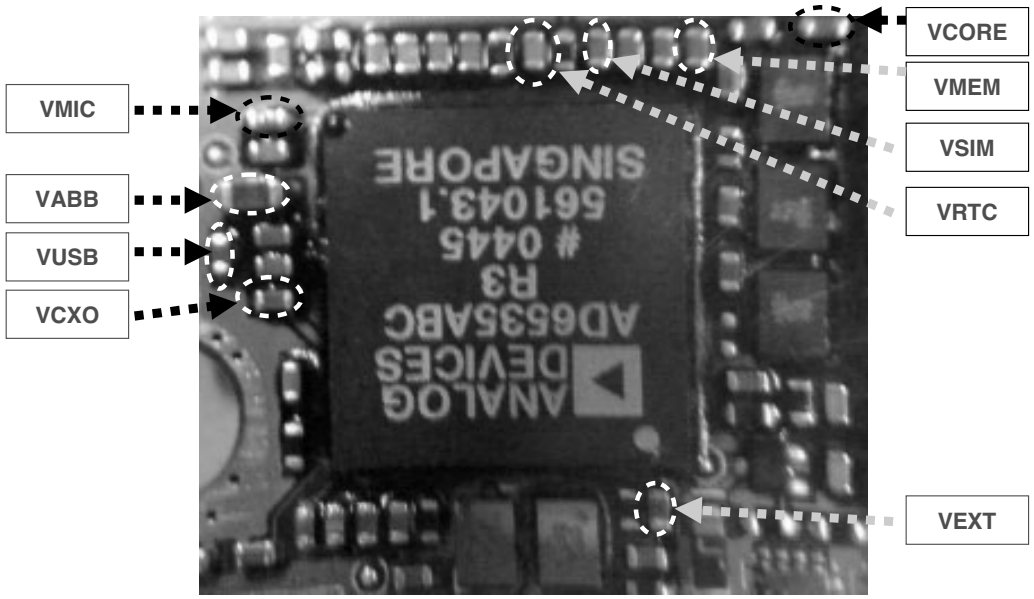
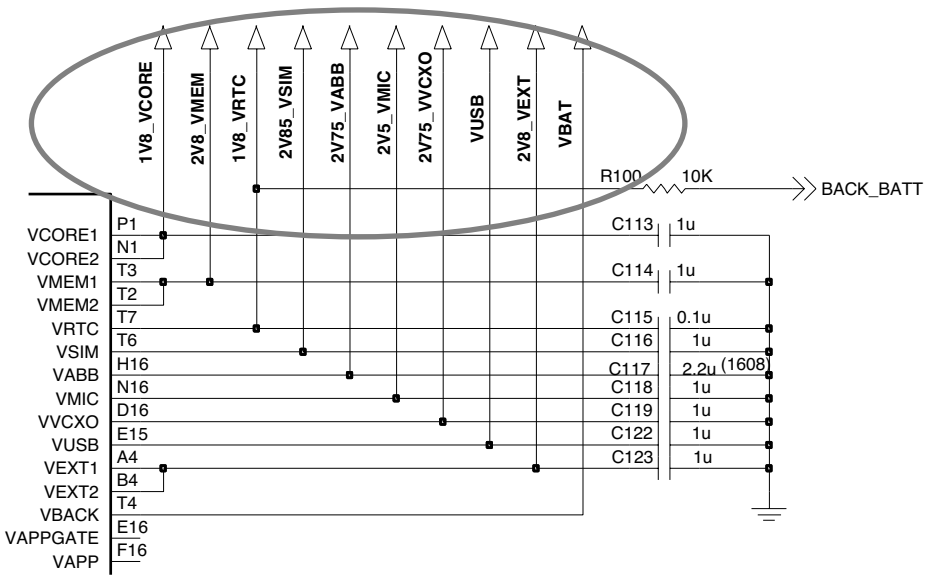


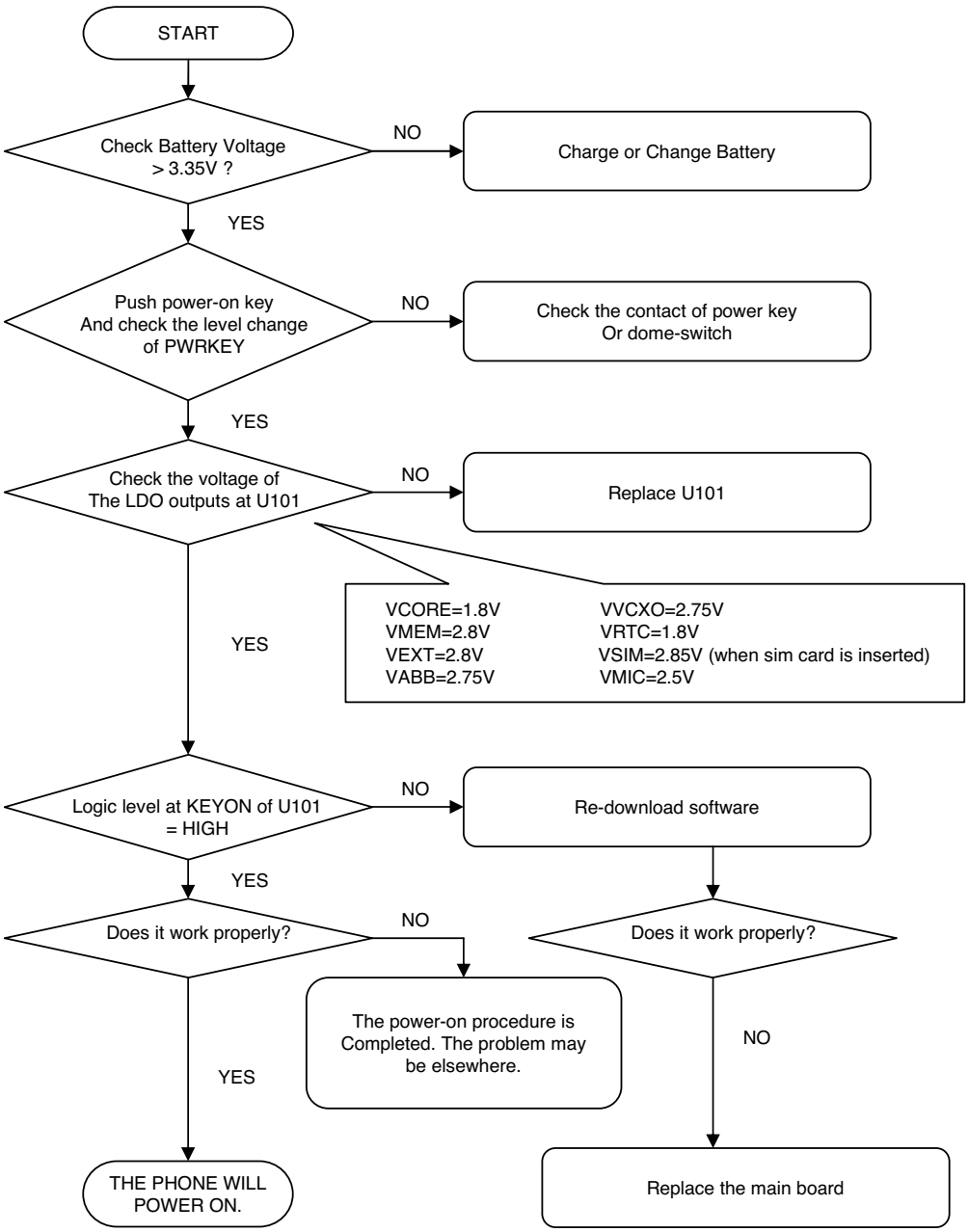
Figure 4-3

CIRCUIT



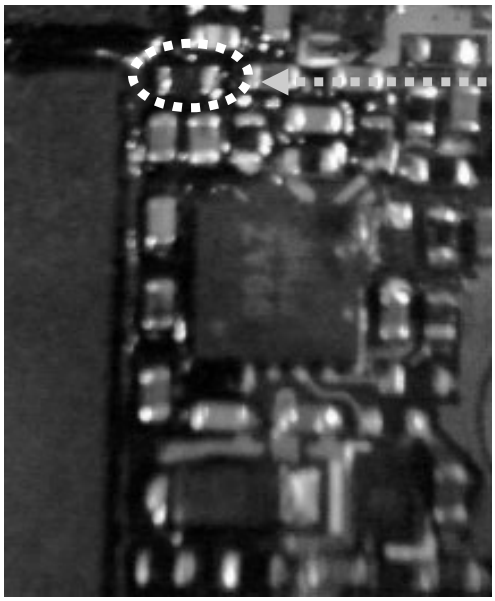
4. TROUBLE SHOOTING

Checking Flow



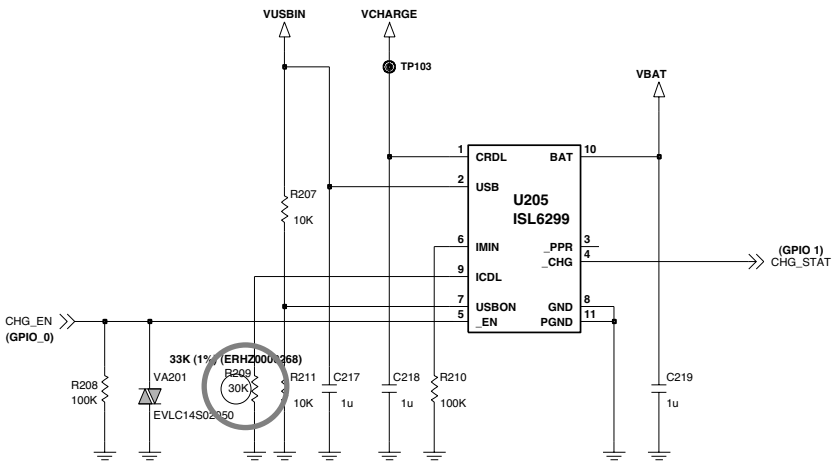
4.4 Charging Trouble

TEST POINT



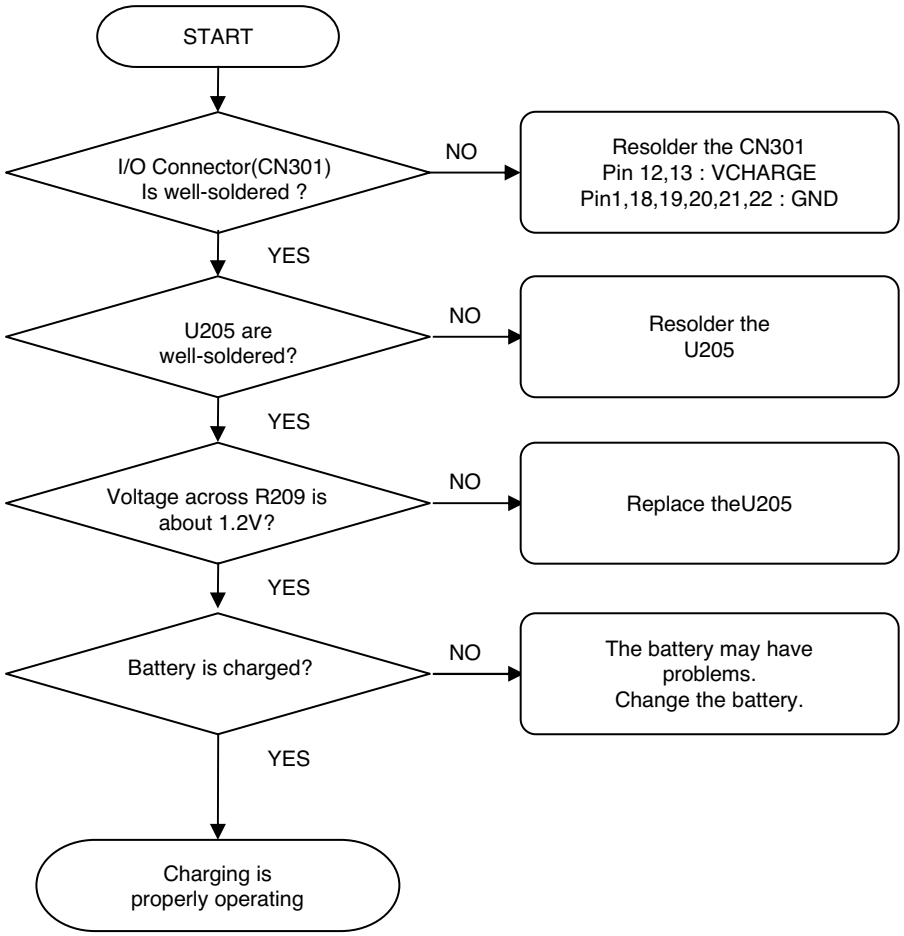
CIRCUIT

Charging IC



4. TROUBLE SHOOTING

Checking Flow



4.5 Vibrator Trouble

TEST POINT

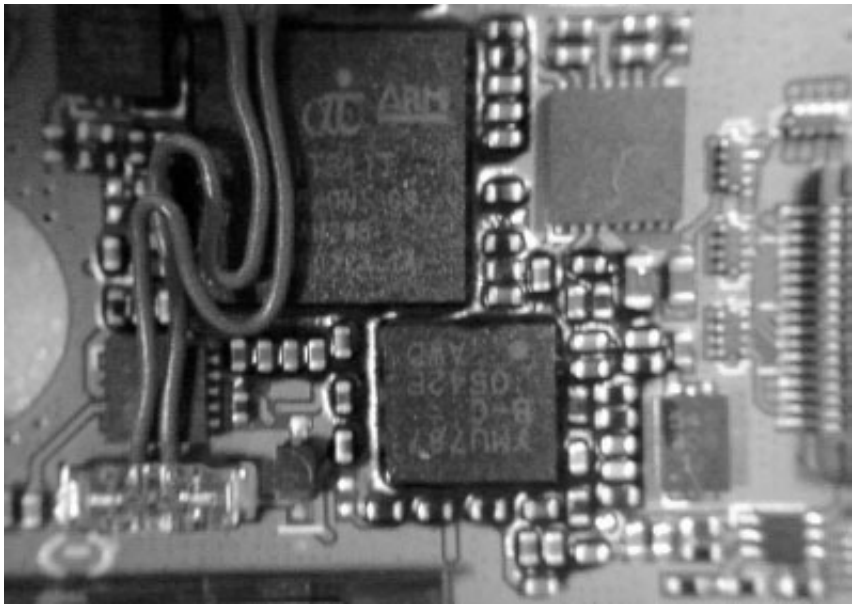
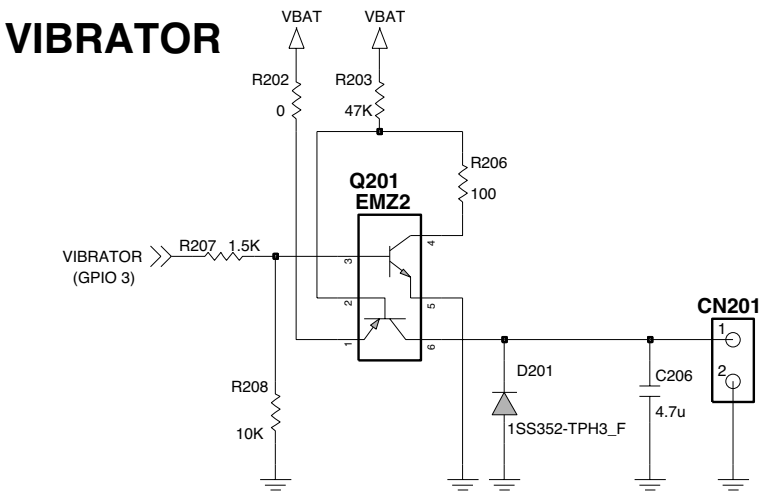


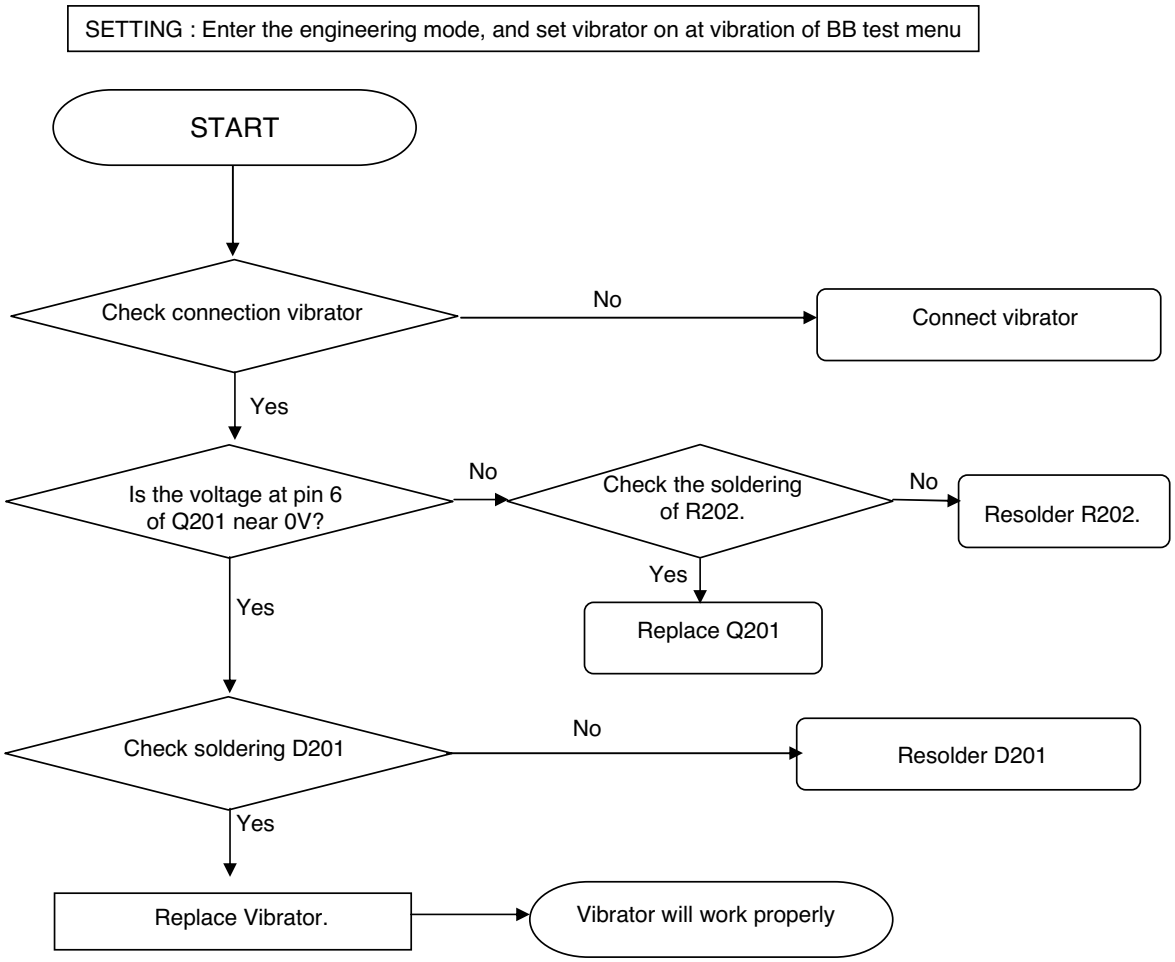
Figure 4-5

CIRCUIT



4. TROUBLE SHOOTING

Checking Flow



4.6 LCD Trouble

TEST POINT

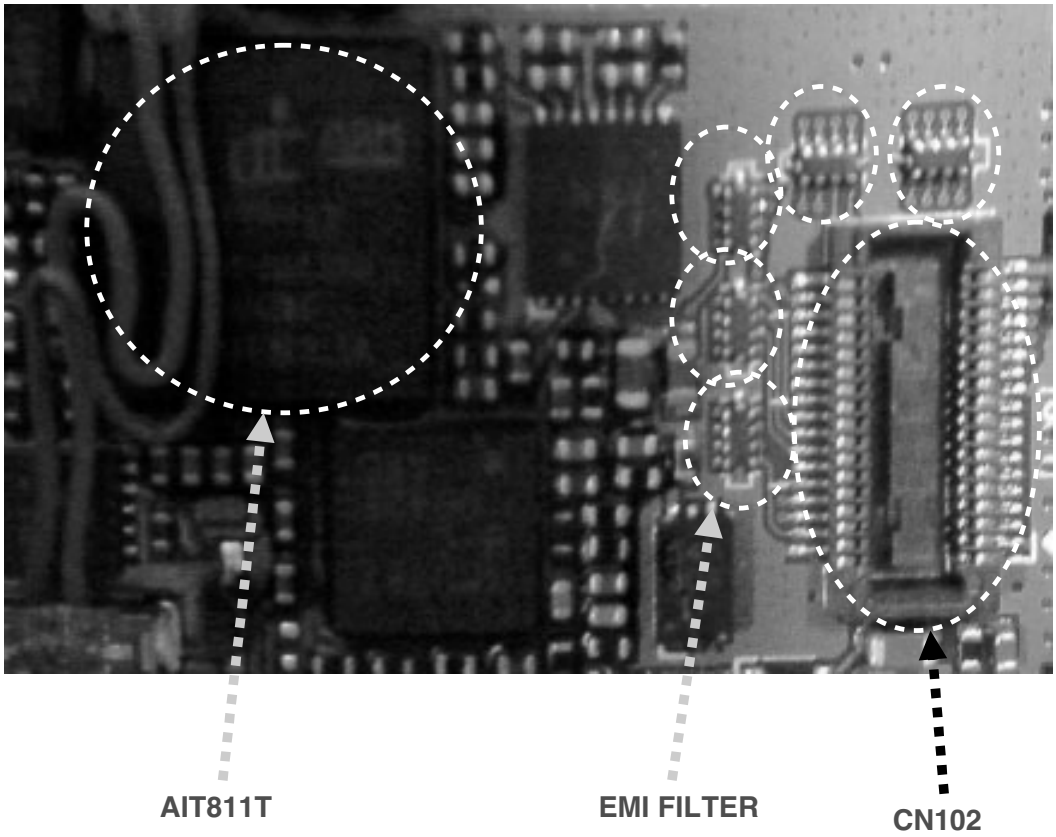
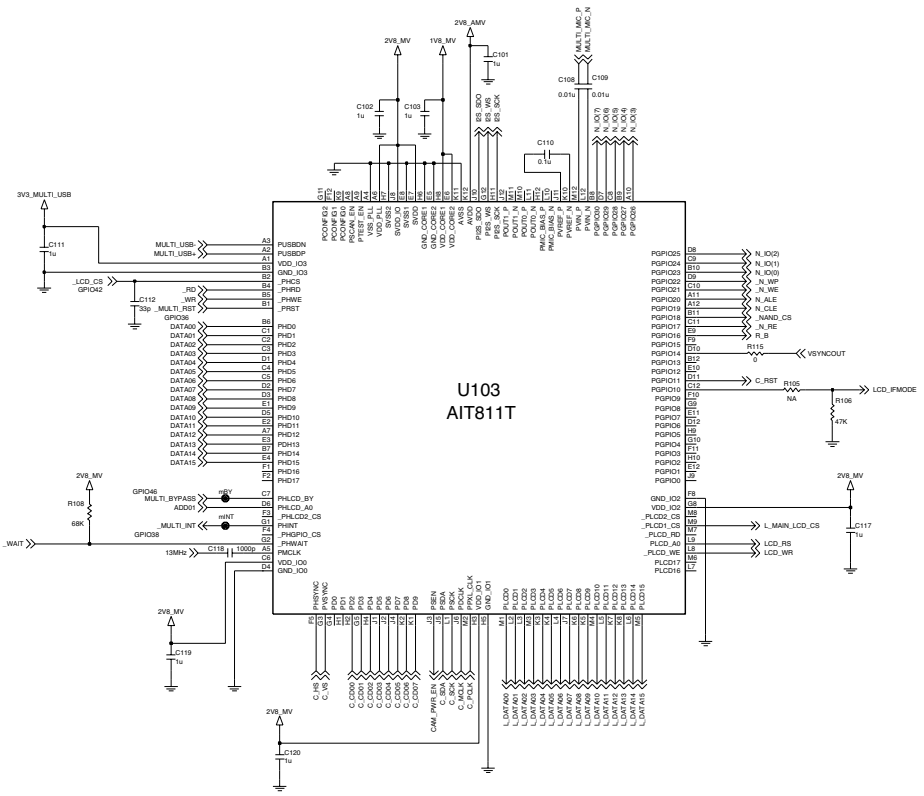


Figure 4-6

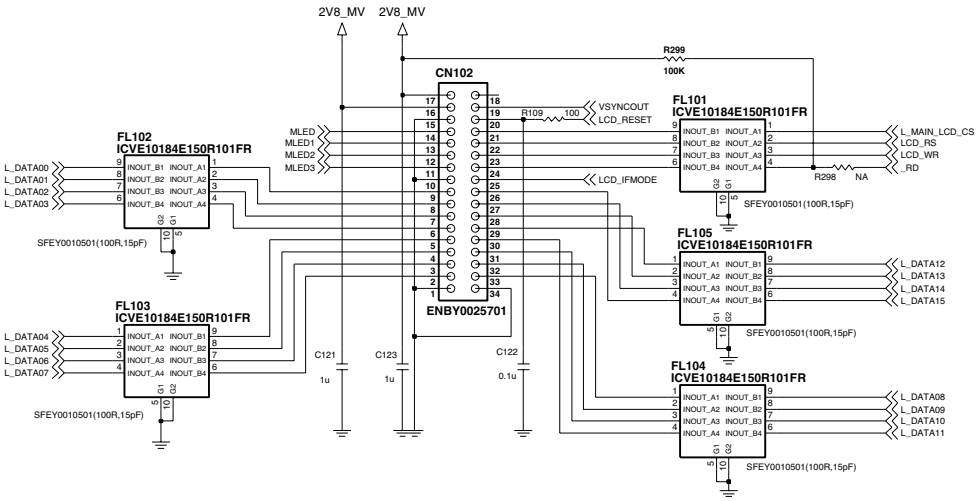
4. TROUBLE SHOOTING

CIRCUIT DIAGRAM

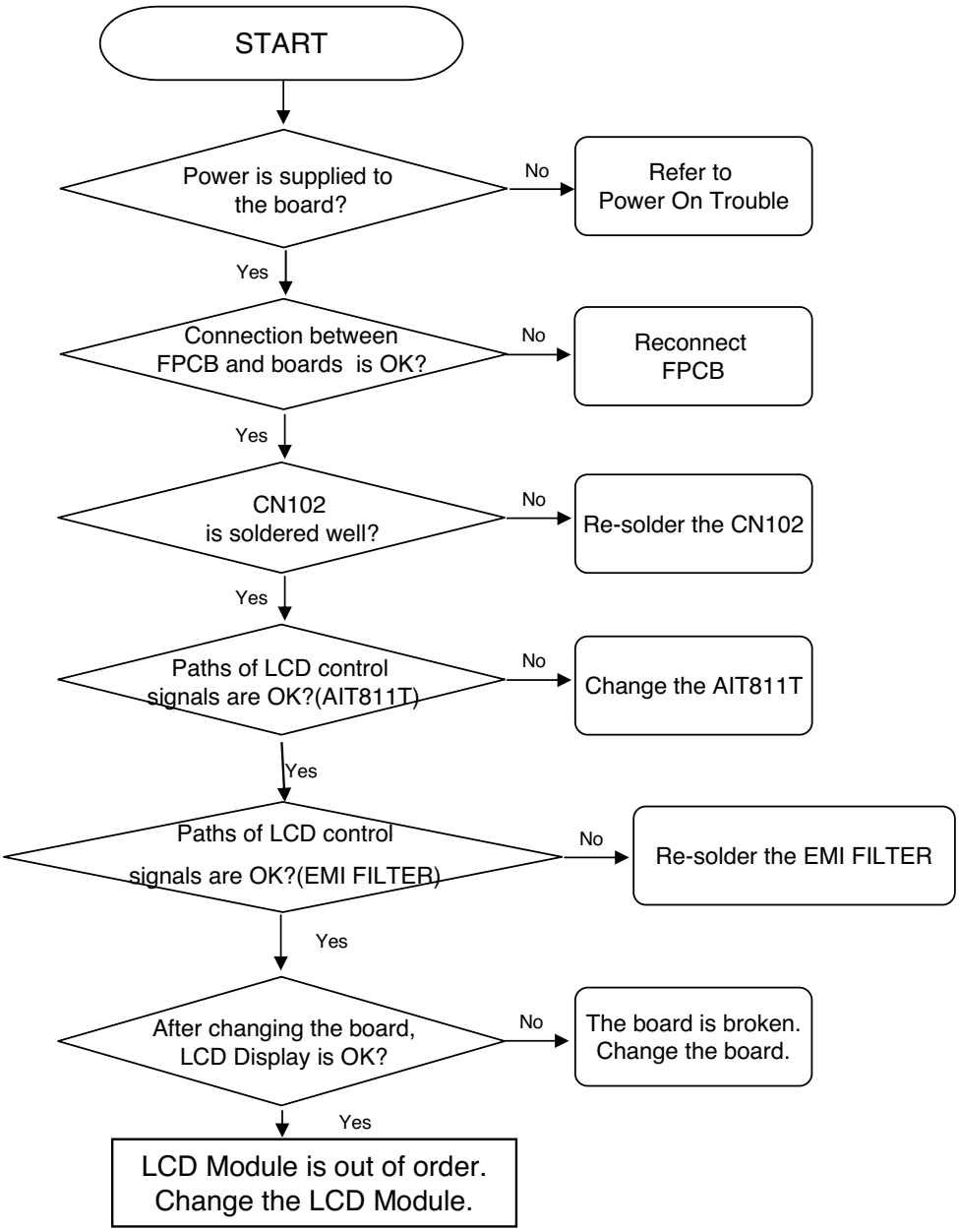


TFT-LCD CONNECTOR

TFT-LCD CONNECTOR



Checking Flow



4.7 BT Trouble

TEST POINT

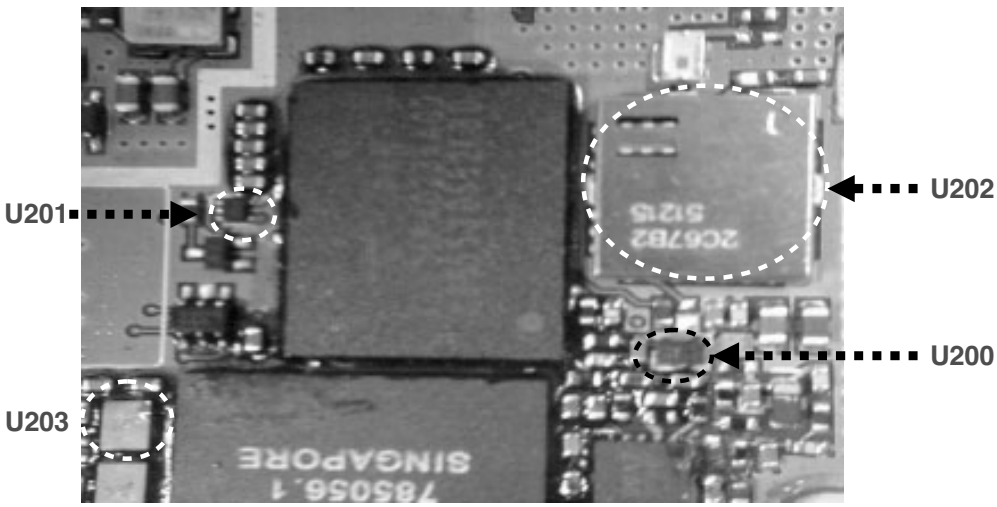
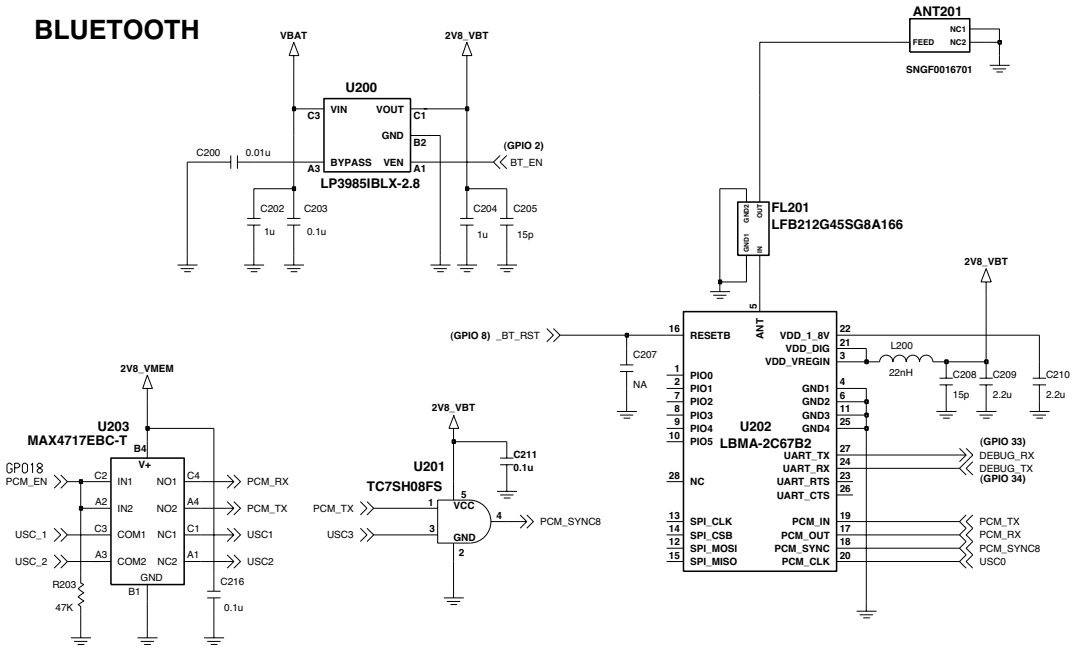
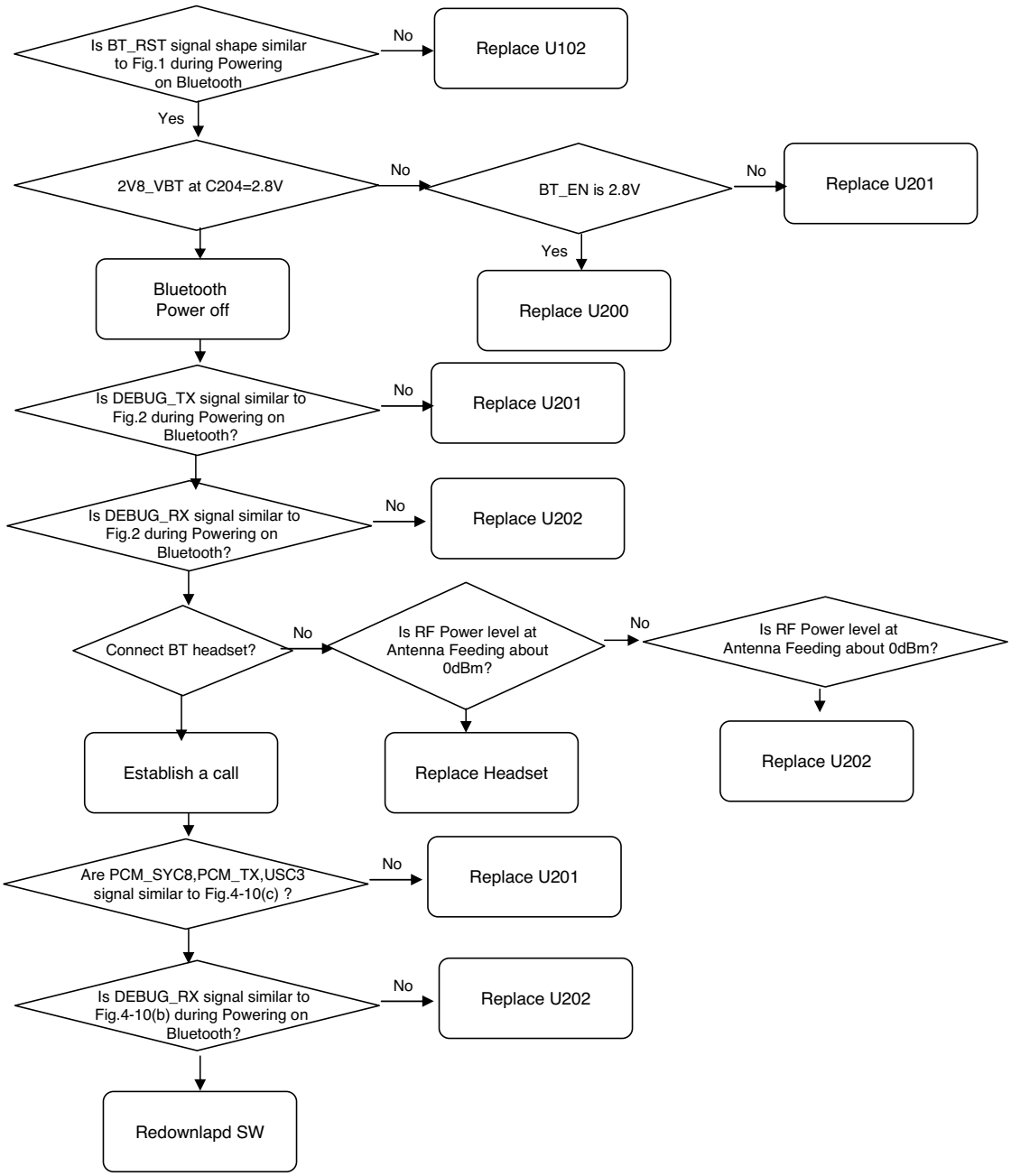


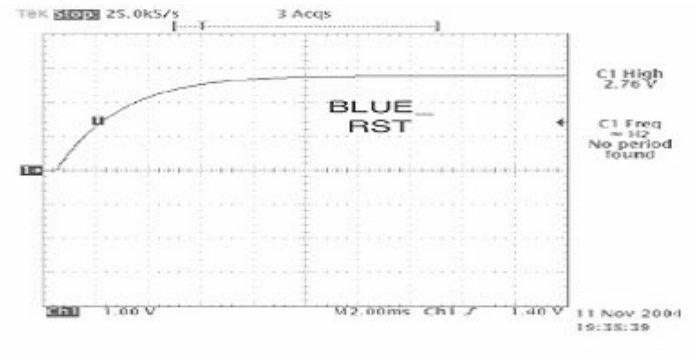
Figure 4-7

CIRCUIT DIAGRAM

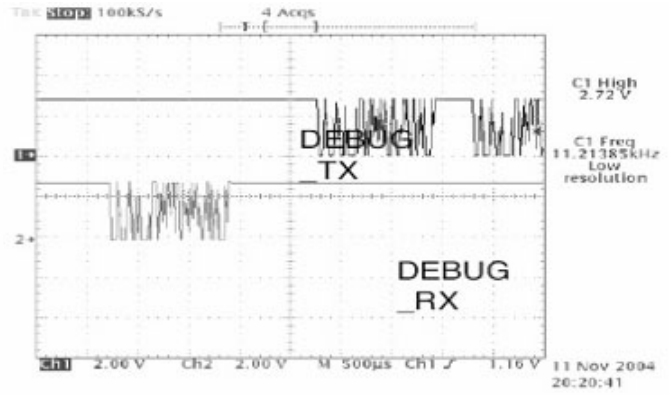


Checking Flow

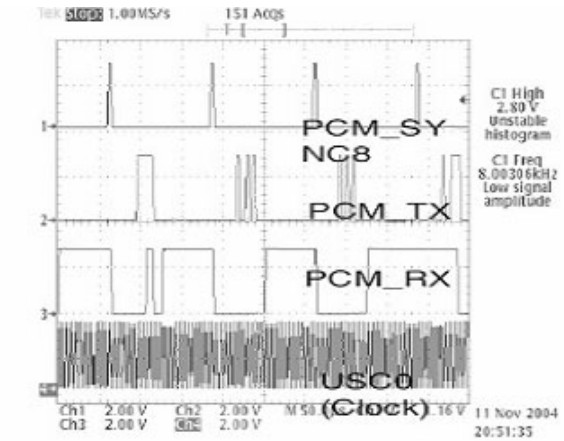




Graph 4-10(a) BLUE-RST



Graph 4-10(b) DEBUG_TX,RX



Graph 4-10(c) PCM_SYNCS,TX,RX,USC0

4.8 Speaker Trouble

TEST POINT

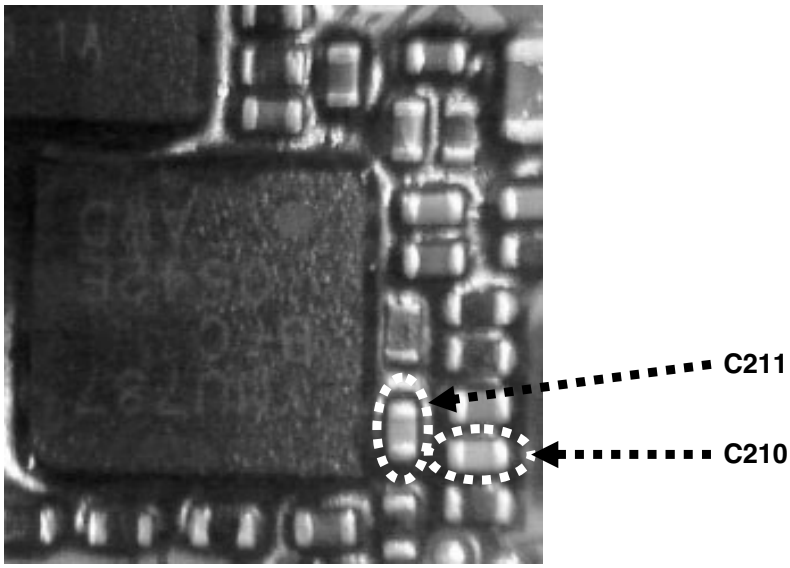
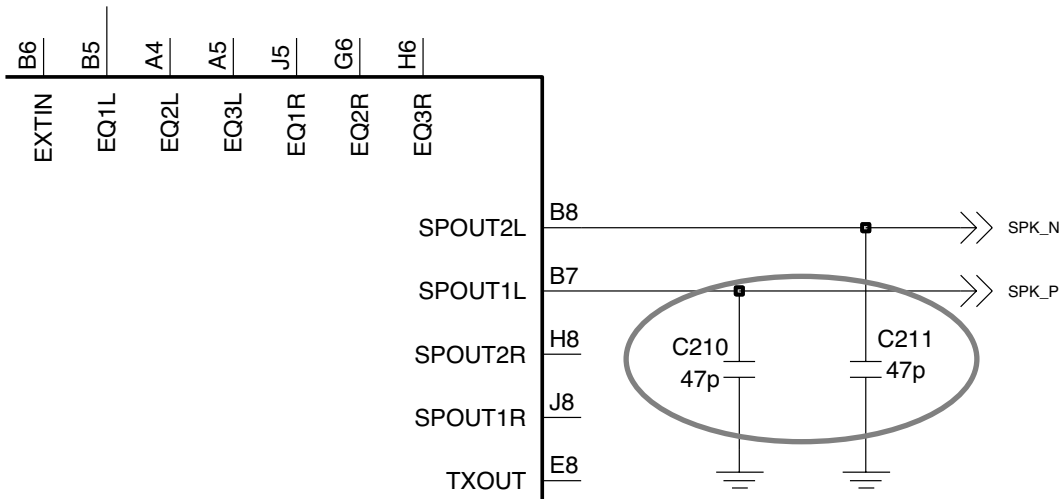


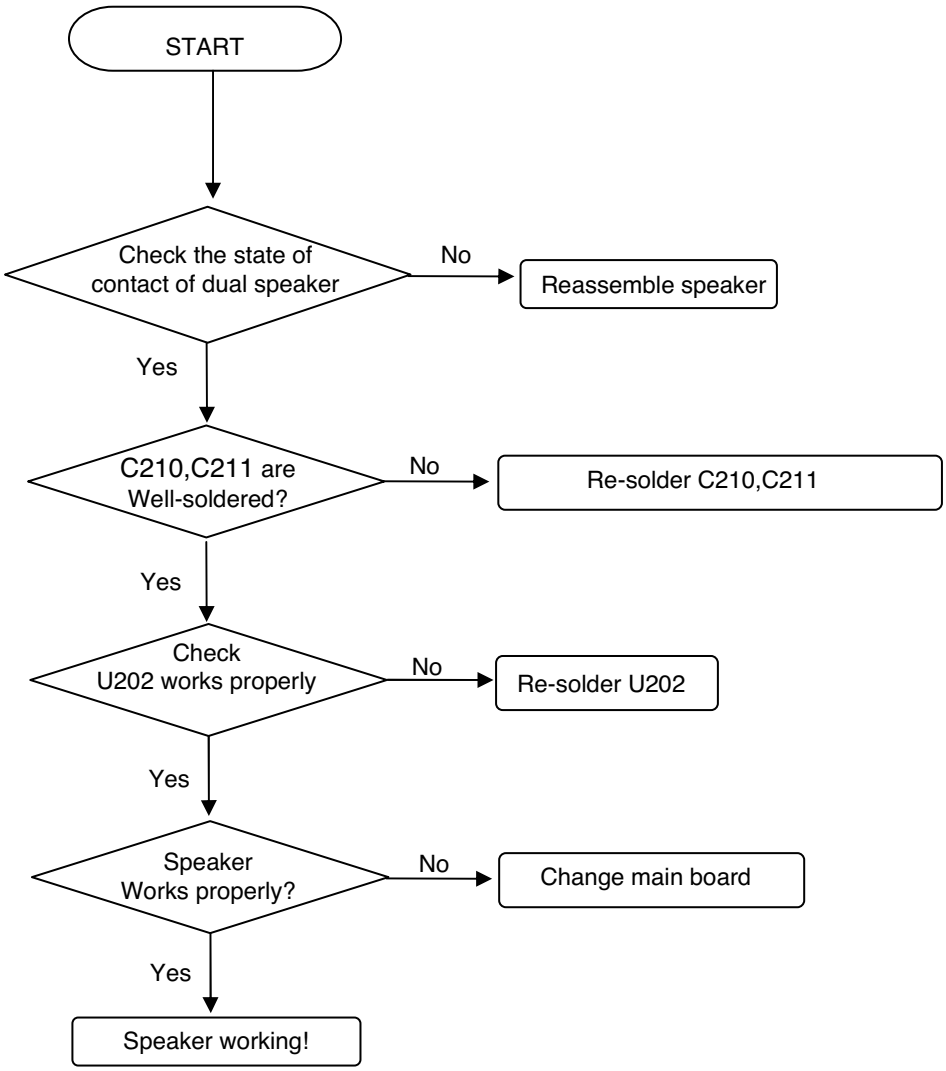
Figure 4-8

CIRCUIT DIAGRAM



4. TROUBLE SHOOTING

Checking Flow



4.9 SIM Card Interface Trouble

TEST POINT

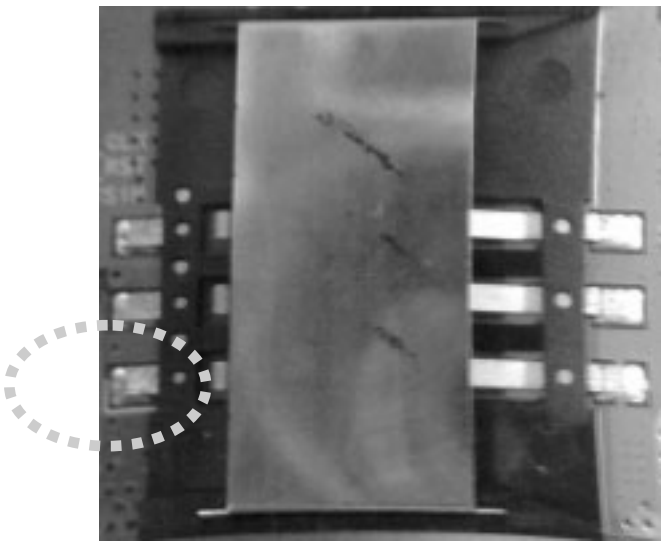
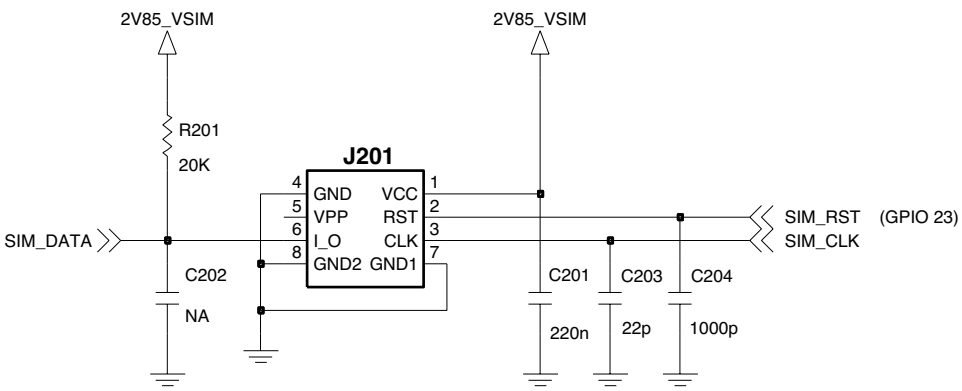


Figure 4-9

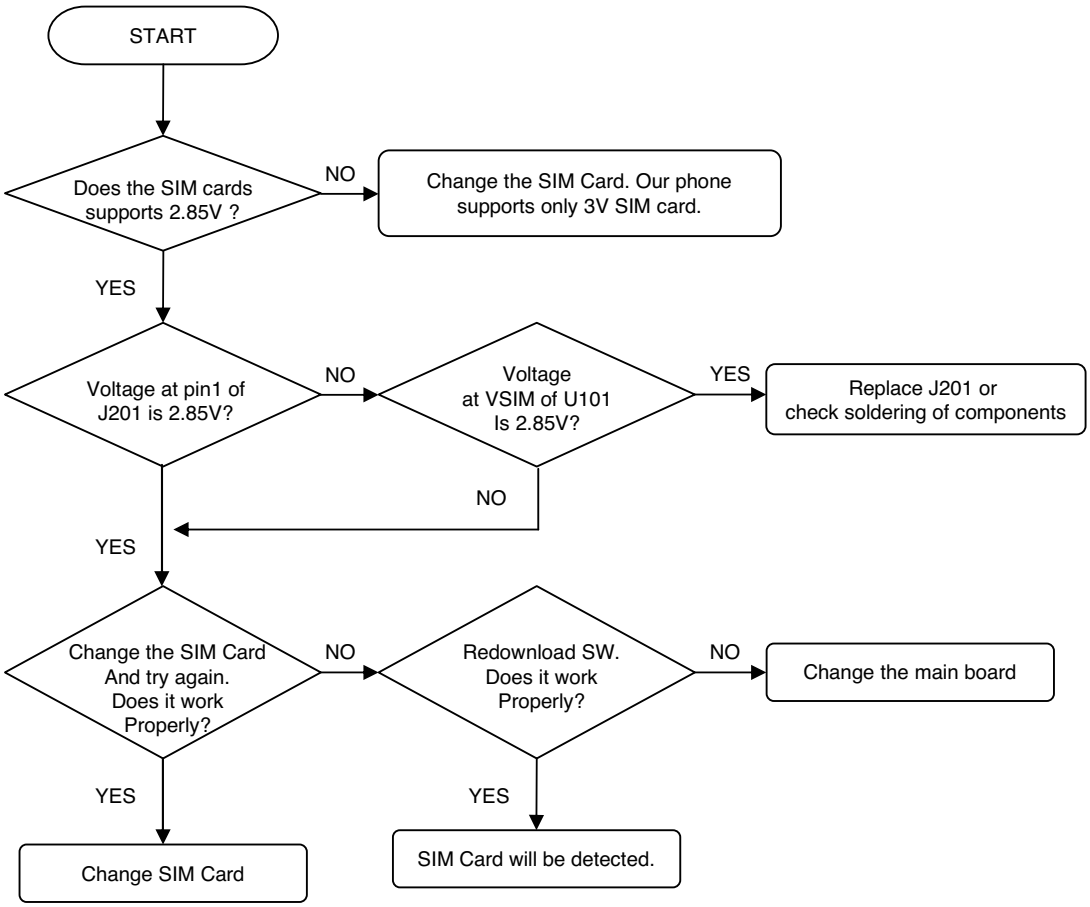
CIRCUIT DIAGRAM

SIM CONNECTOR



4. TROUBLE SHOOTING

Checking Flow



4.10 Earphone Trouble

TEST POINT

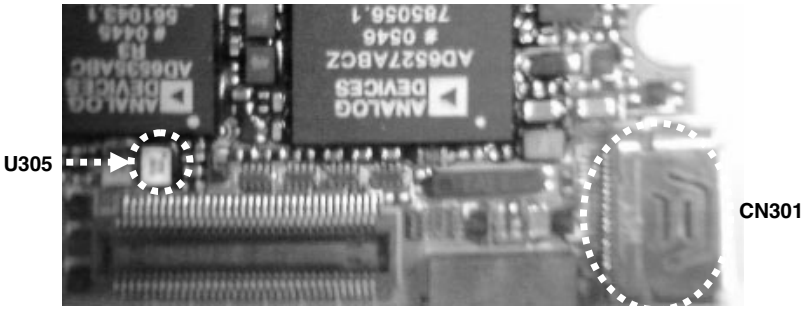
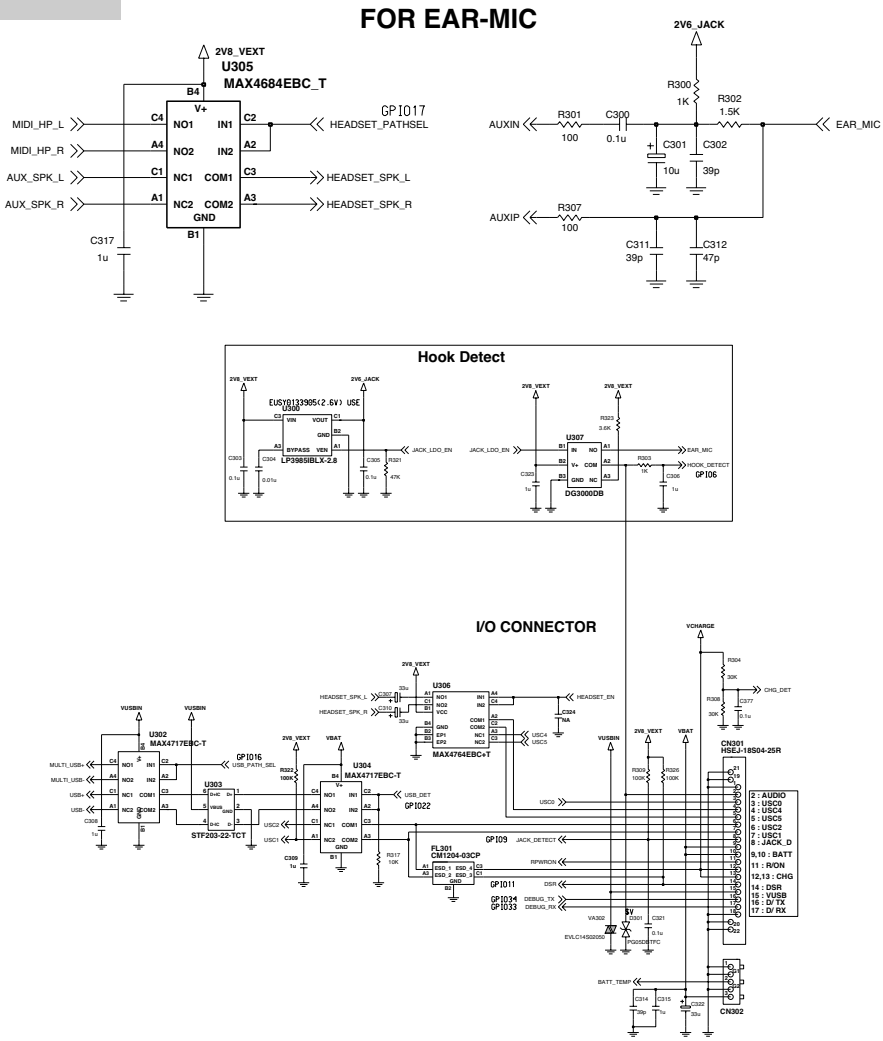


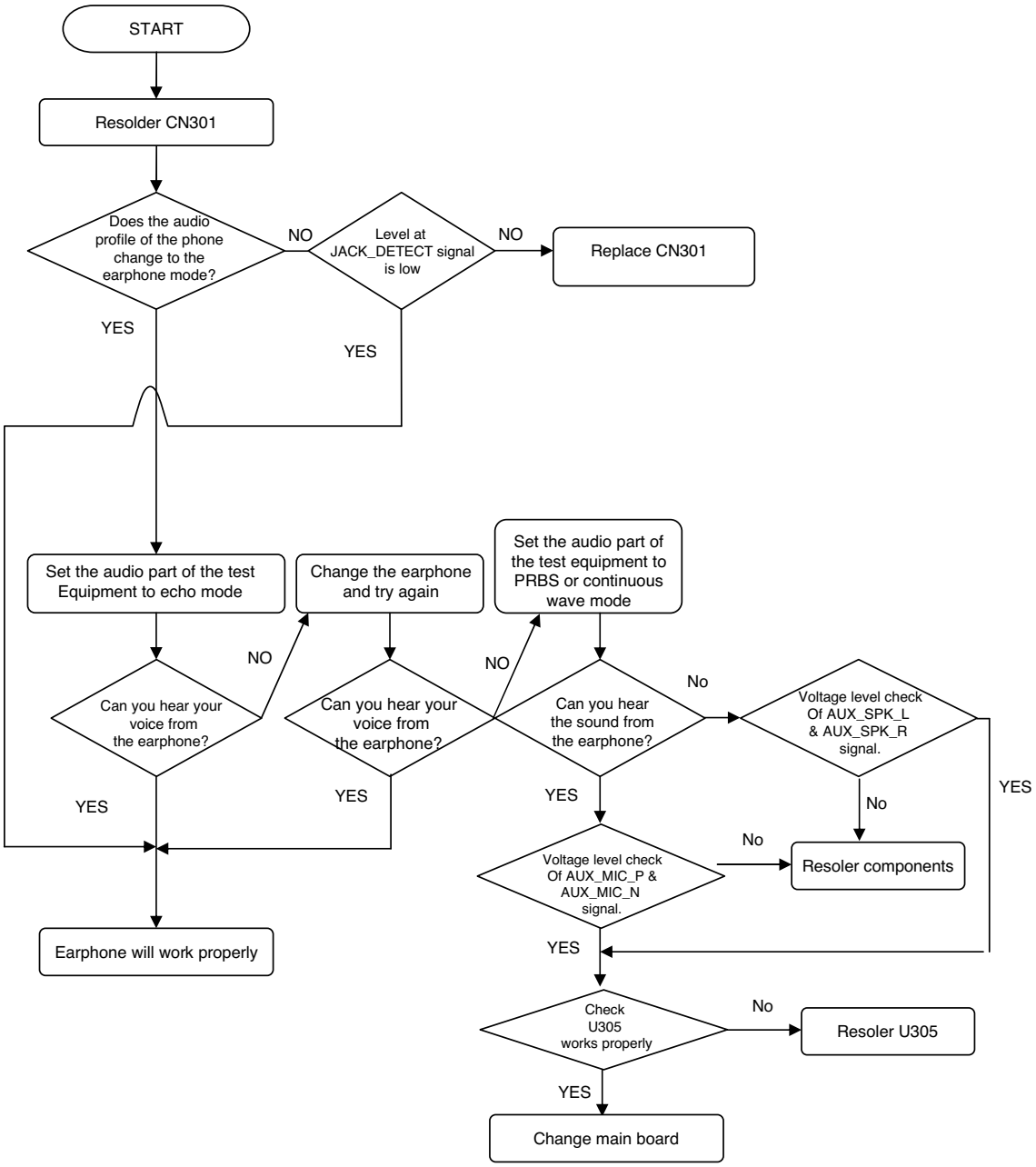
Figure 4-10

CIRCUIT DIAGRAM



4. TROUBLE SHOOTING

Checking Flow



4.11 Receiver Trouble

TEST POINT

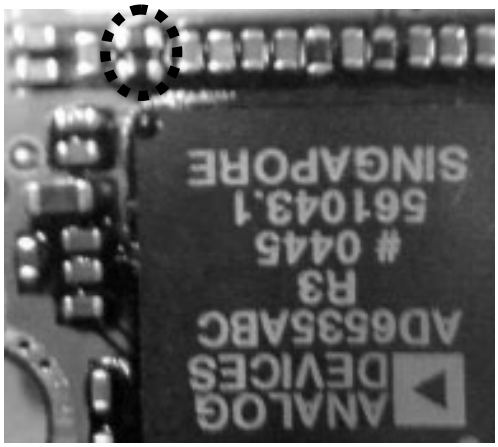
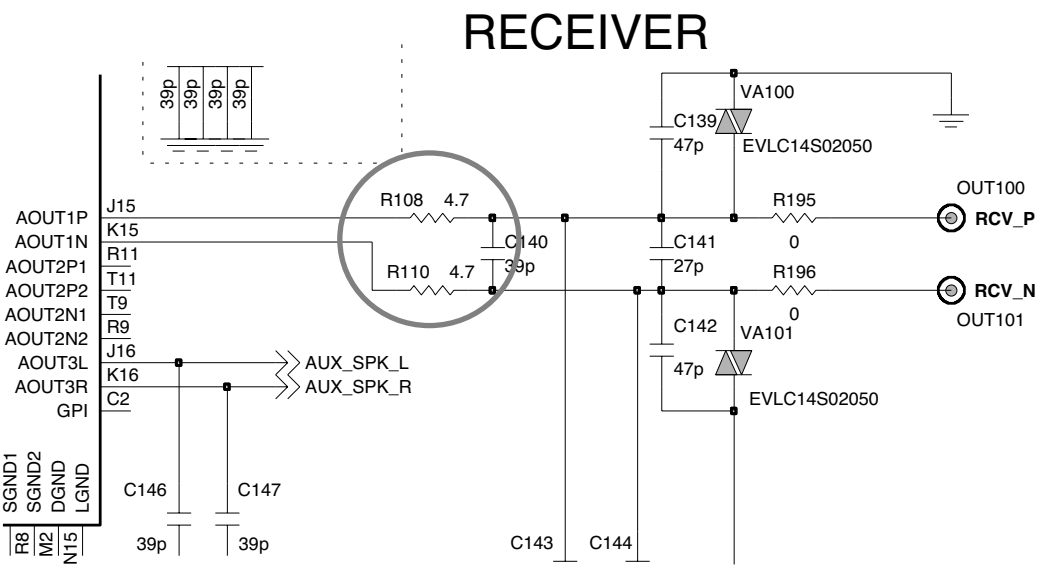


Figure 4-13

CIRCUIT DIAGRAM

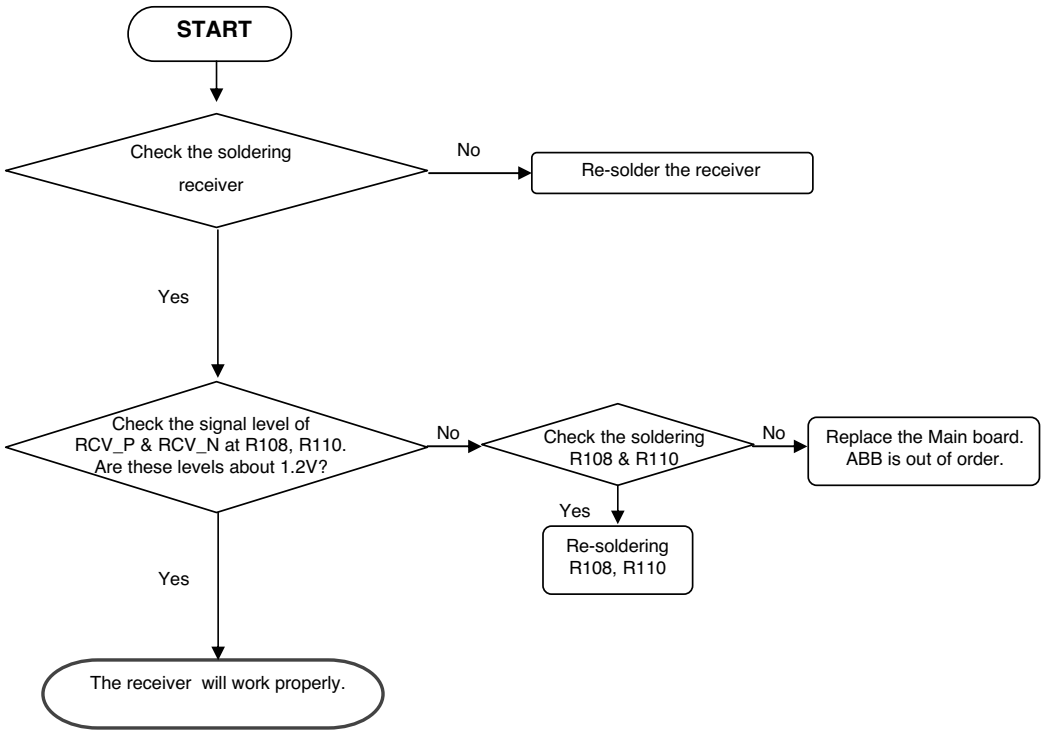


4. TROUBLE SHOOTING

Checking Flow

SETTING : After initialize Agilent 8960, Test EGSM, DCS, PCS mode

Set the property of audio as PRBS or continuous wave. Set the receiving volume of mobile as Max.



4.12 Microphone Trouble

TEST POINT

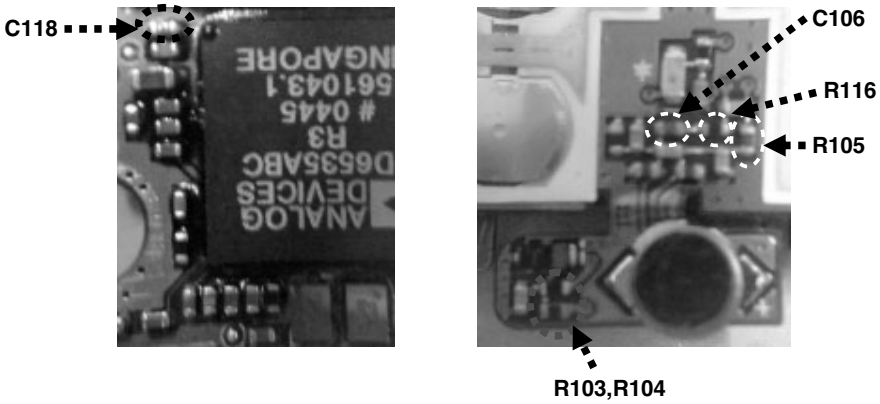
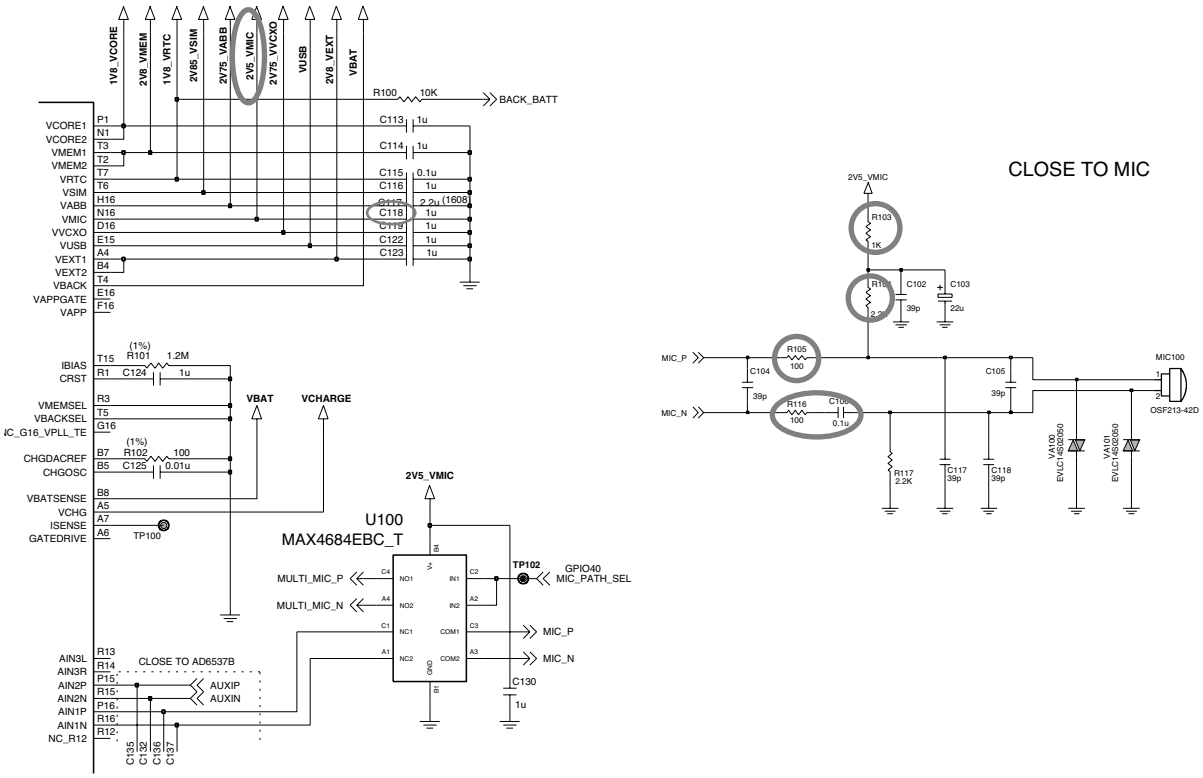


Figure 4-14

CIRCUIT DIAGRAM

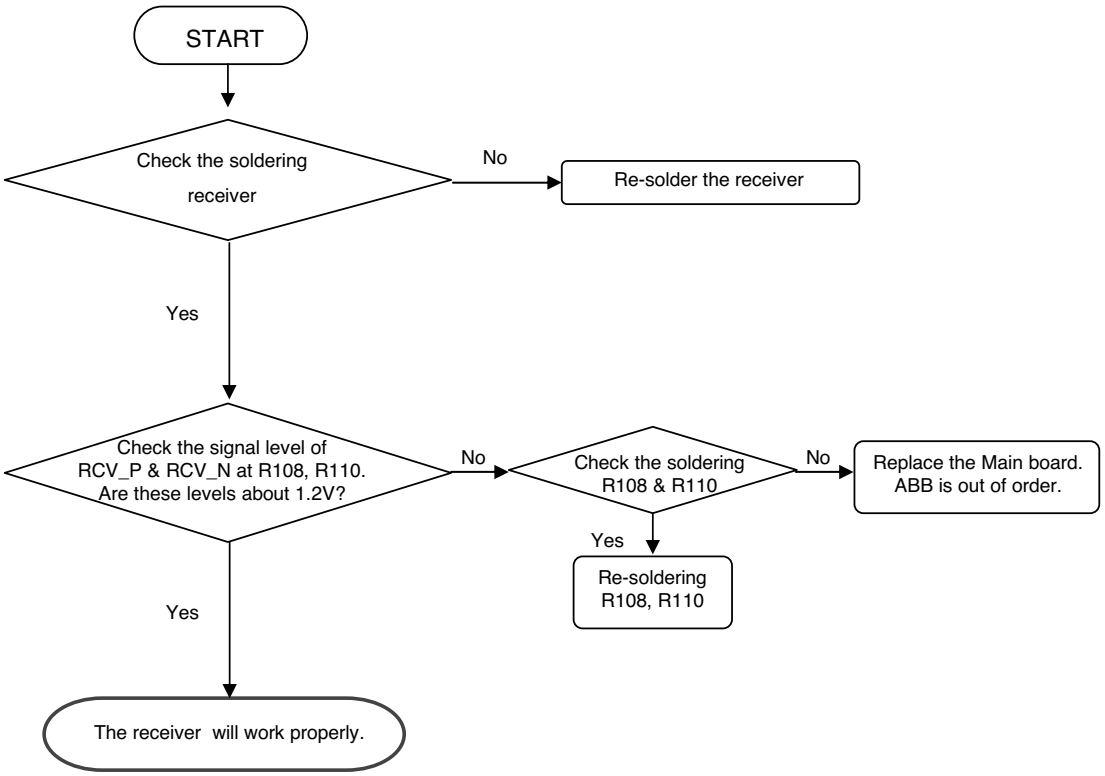


4. TROUBLE SHOOTING

Checking Flow

SETTING : After initialize Agilent 8960, Test EGSM, DCS, PCS mode

Set the property of audio as PRBS or continuous wave. Set the receiving volume of mobile as Max.



4.13 RTC Trouble

TEST POINT

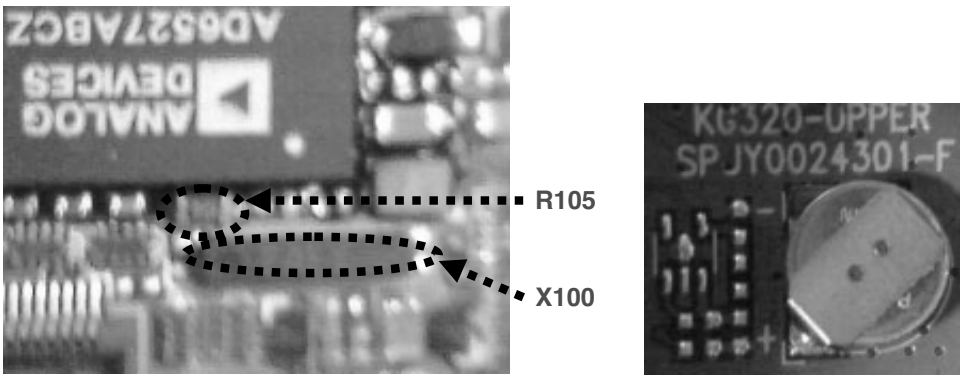
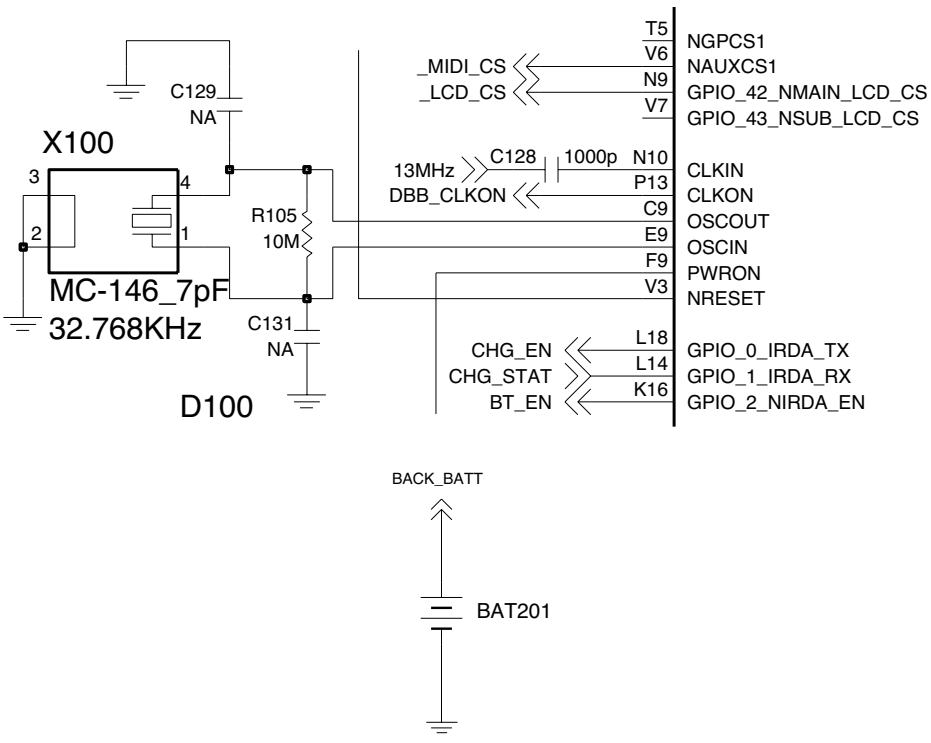


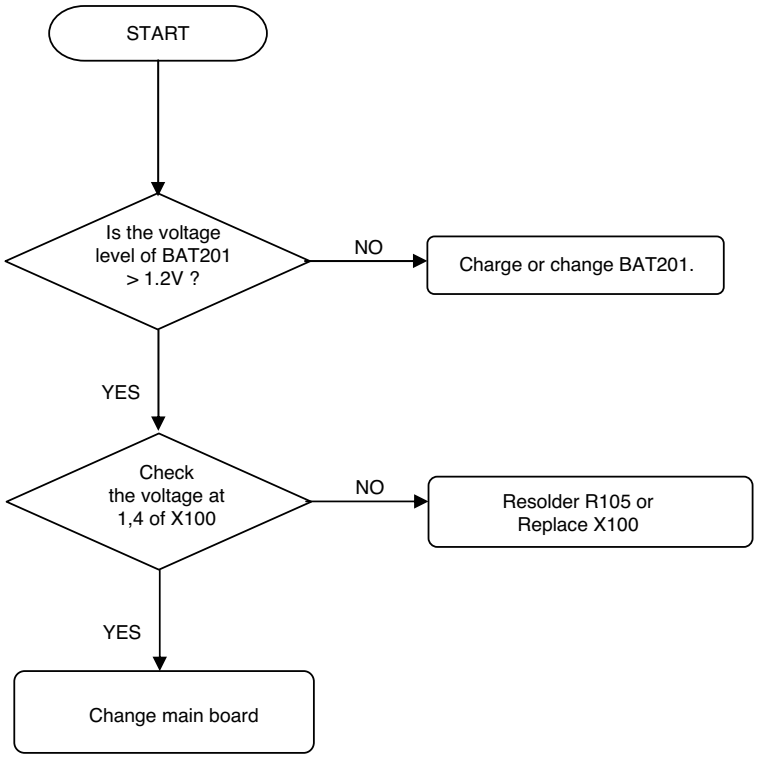
Figure 4-15

CIRCUIT DIAGRAM



4. TROUBLE SHOOTING

Checking Flow



4.14 Camera and Flash Trouble

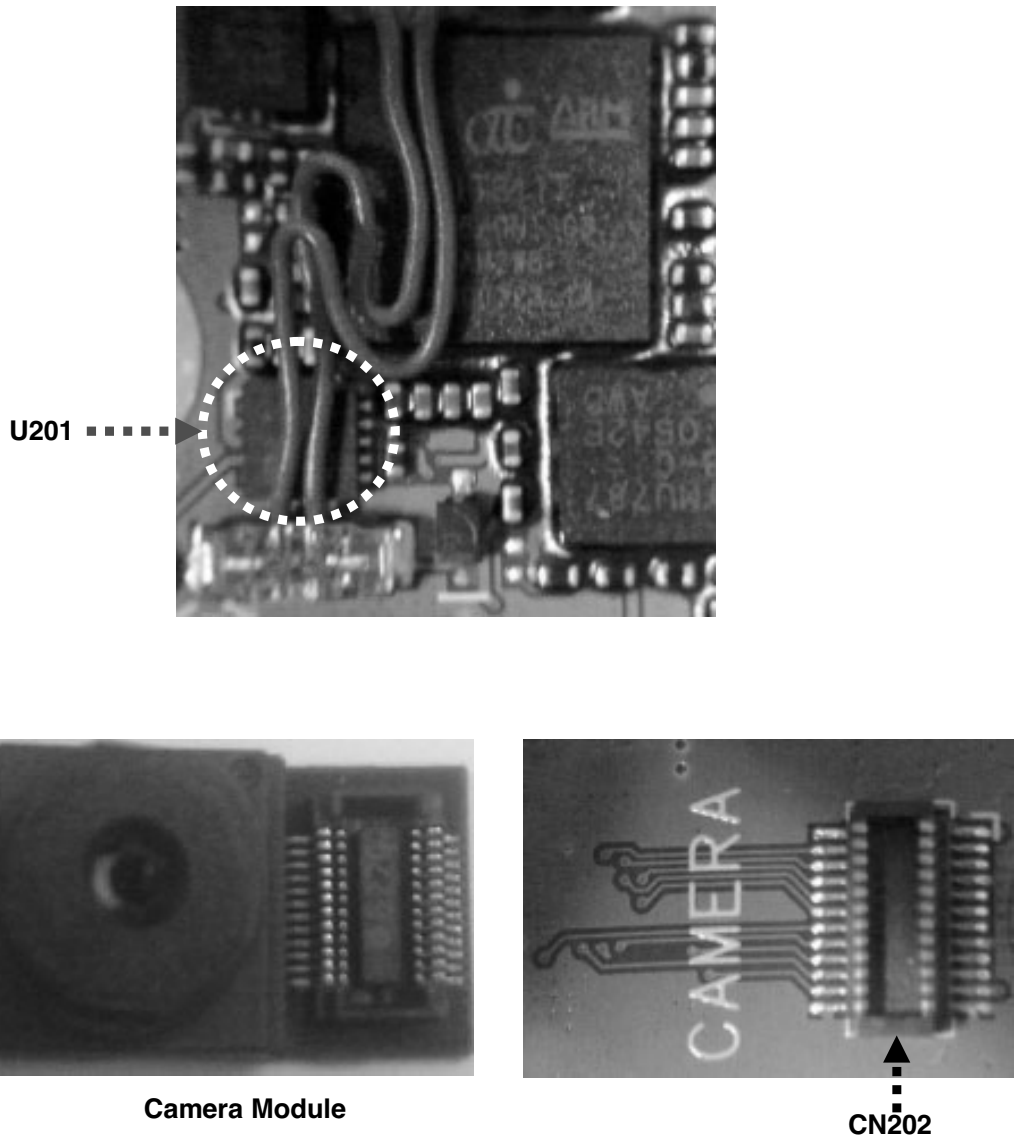
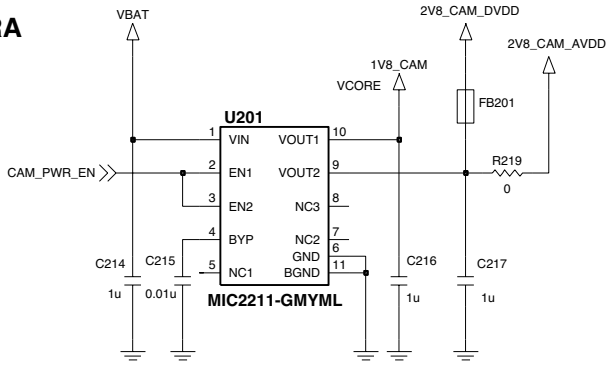


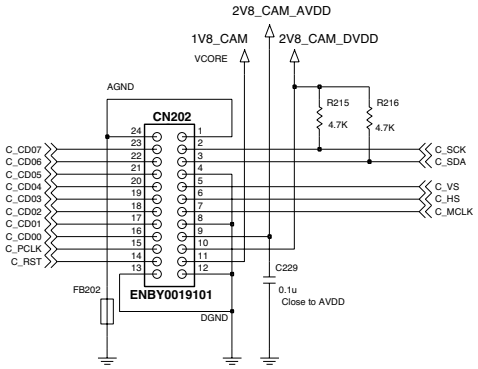
Figure 4-17

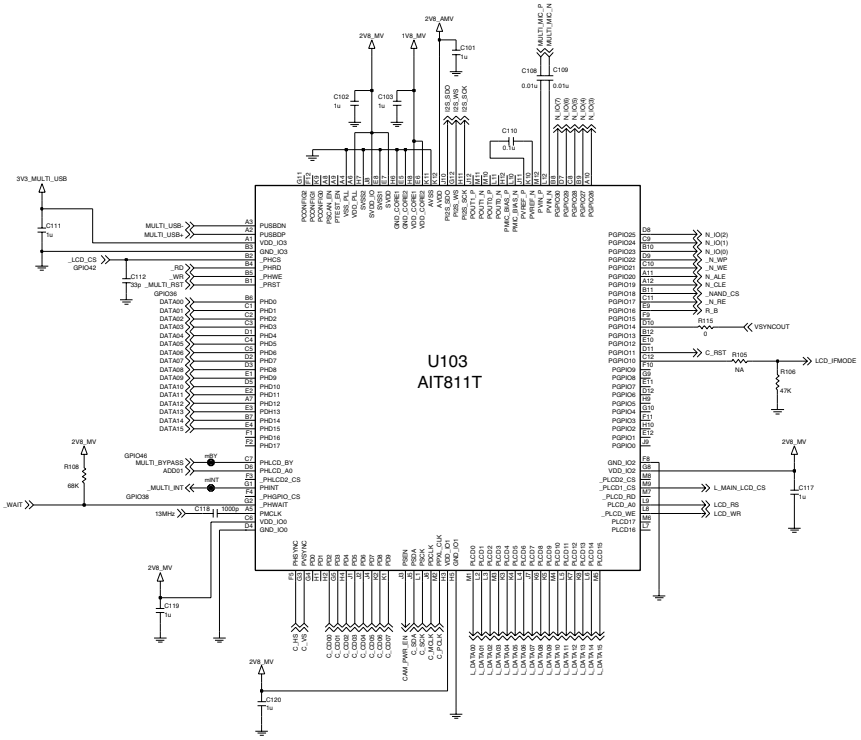
4. TROUBLE SHOOTING

Circuit Diagram

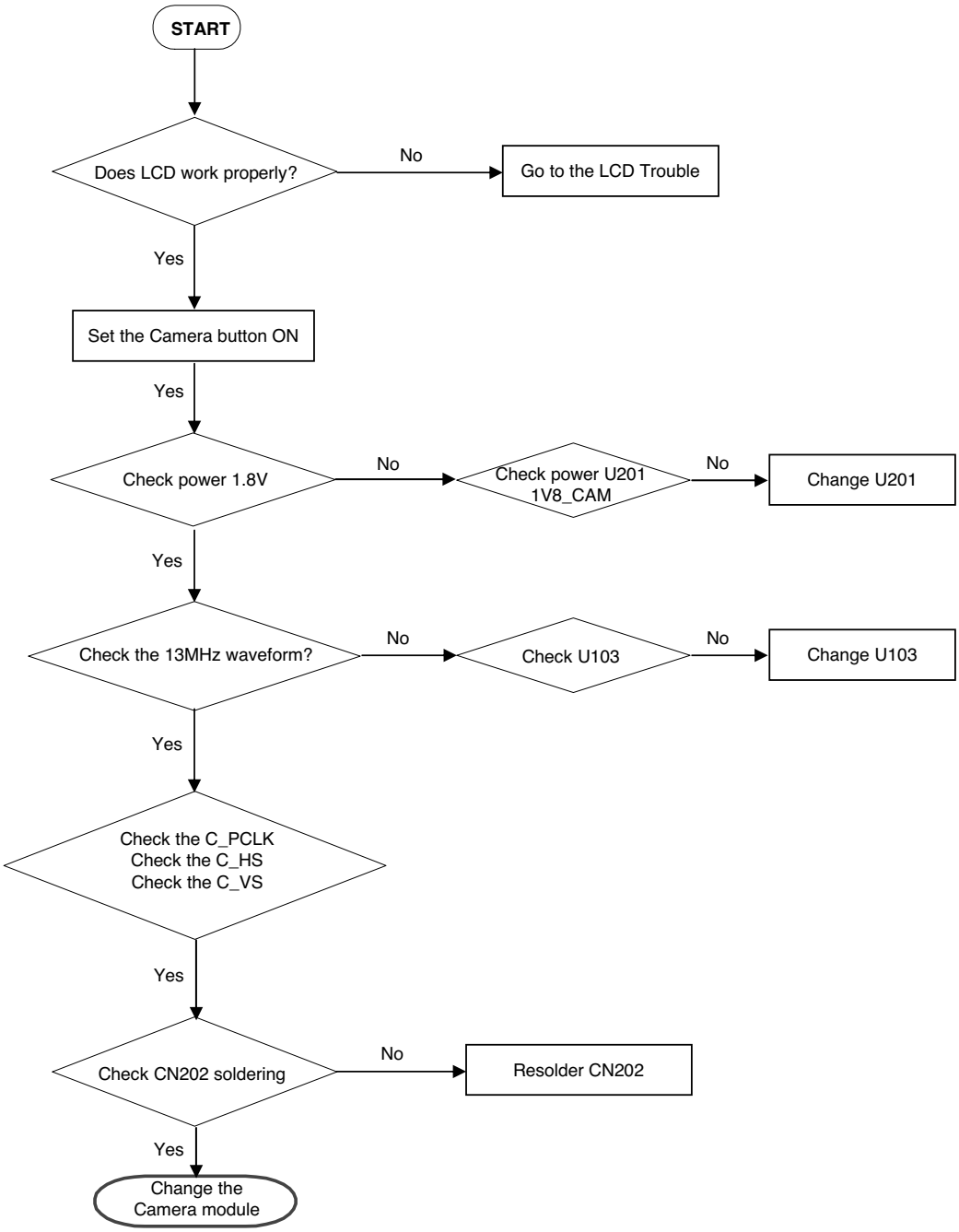
1.3 Pixel CAMERA







Checking Flow



5. DOWNLOAD AND CALIBRATION

5.1 Download

A. Download Setup

Figure 5-1 describes Download setup

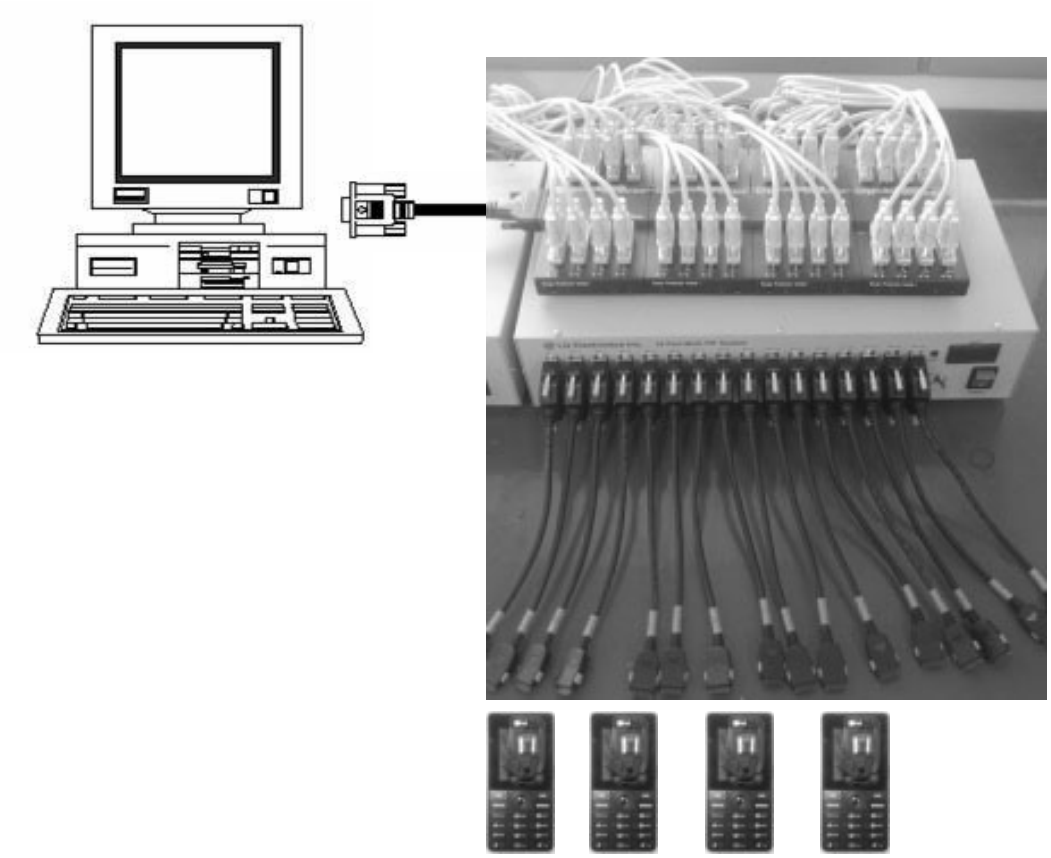
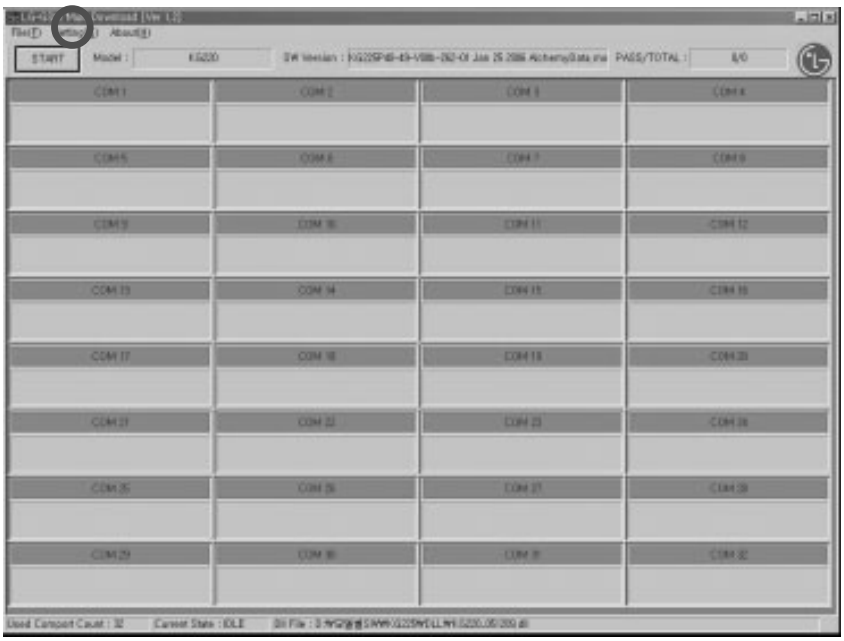


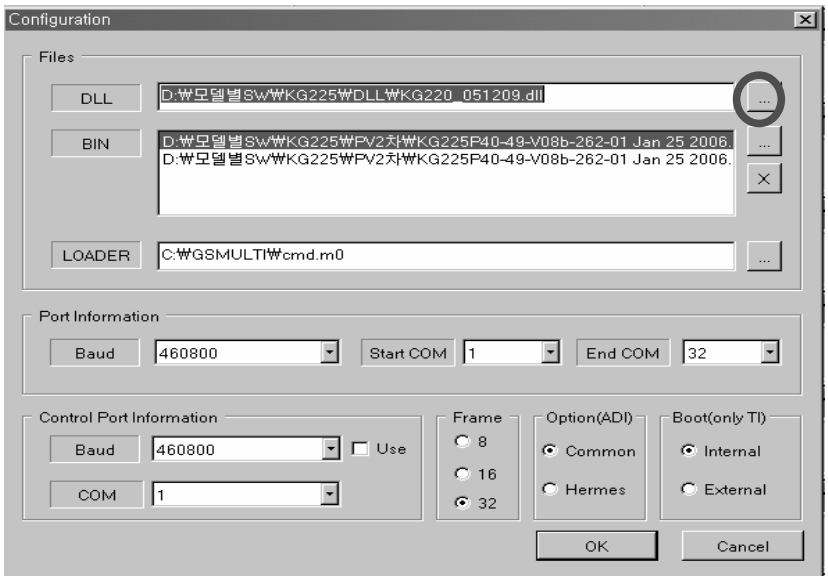
Figure 5-1. Download Setup

B. Download Procedure

1. Run GSM Multi Download program and select Setting

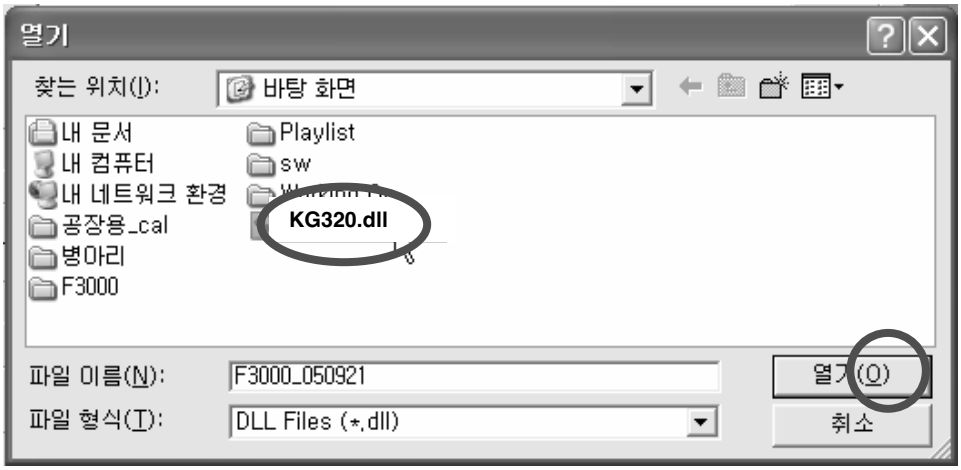


2. Select Configuration from the menu and you may see this window.



5. DOWNLOAD AND CALIBRATION

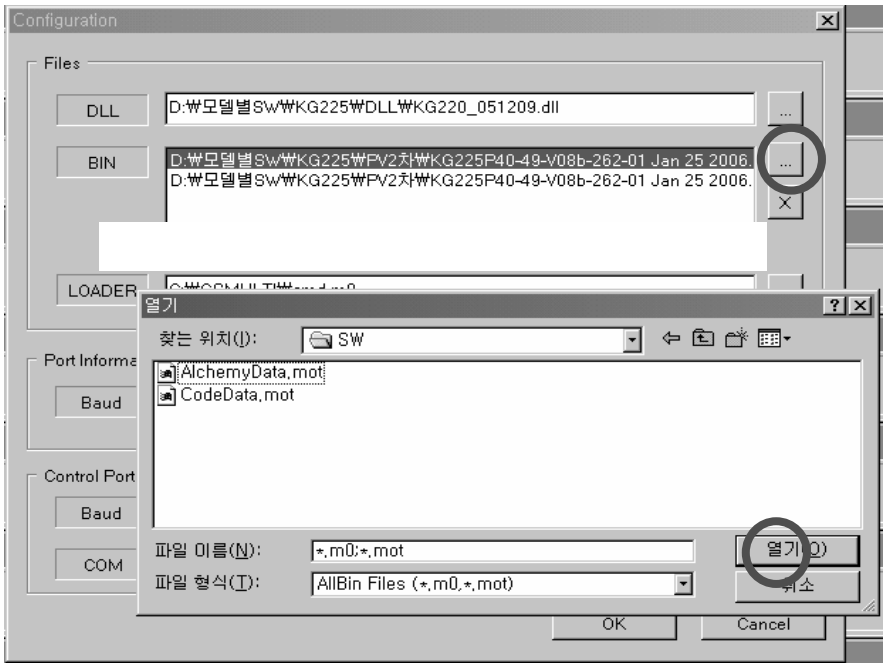
3. Press [...] key to select DLL file and press Open



4. Press [...] key to select the mot files

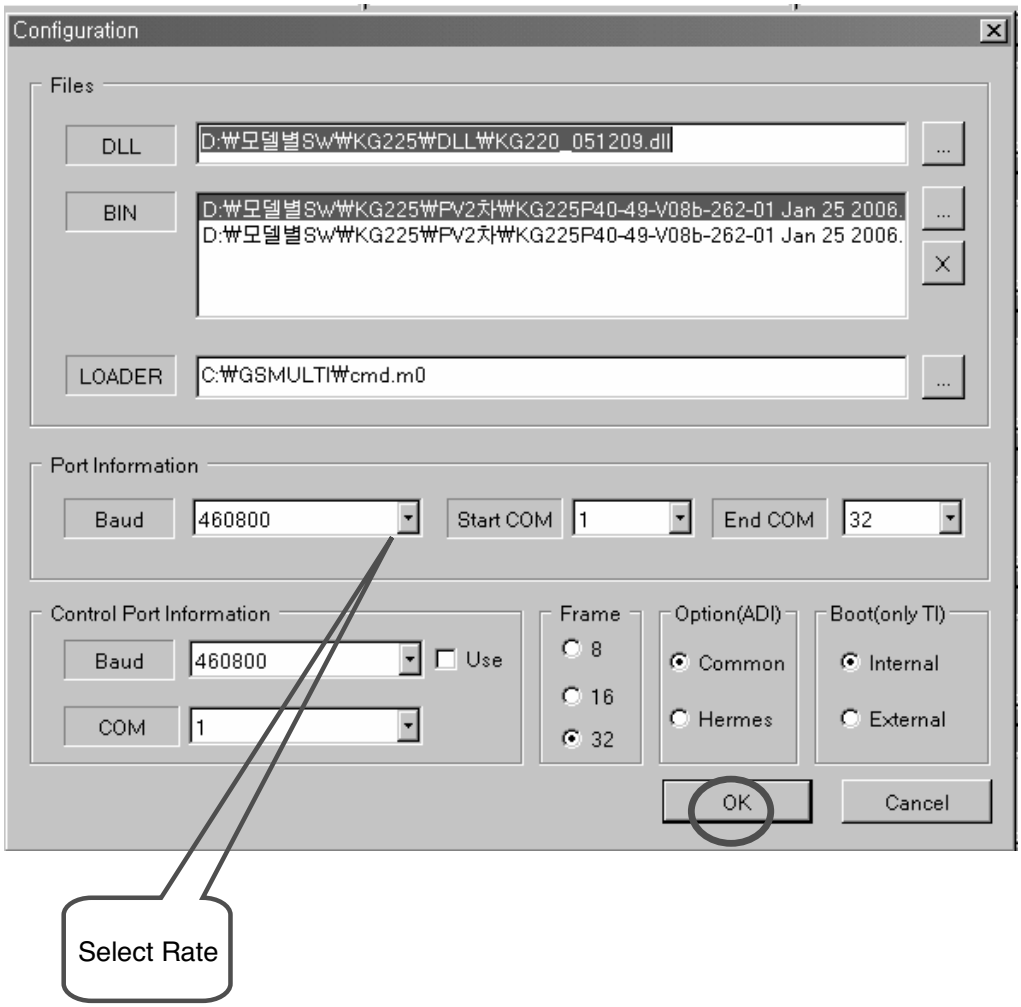
5. Select AlchemyData.mot and press open

6. Repeat step 4-5 to select CodeData.mot



7. Check if the ADI option is set to Hermes

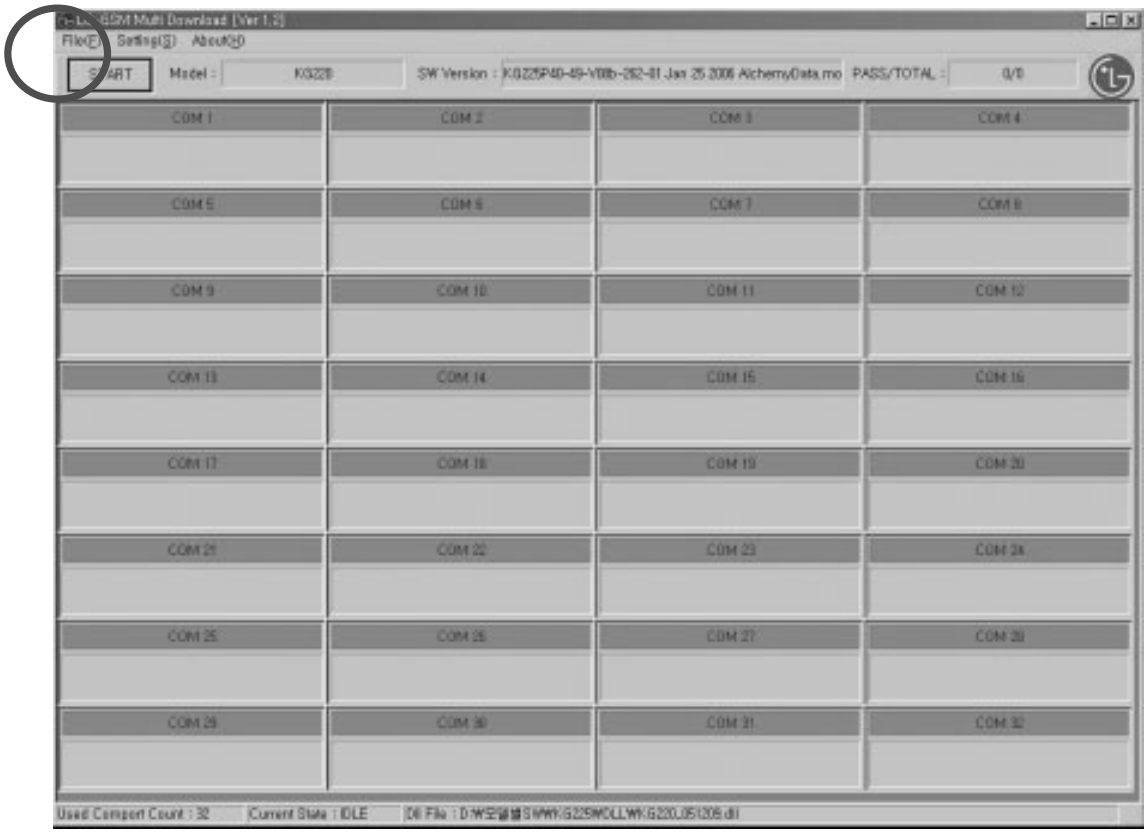
8. Press OK to end Configuration



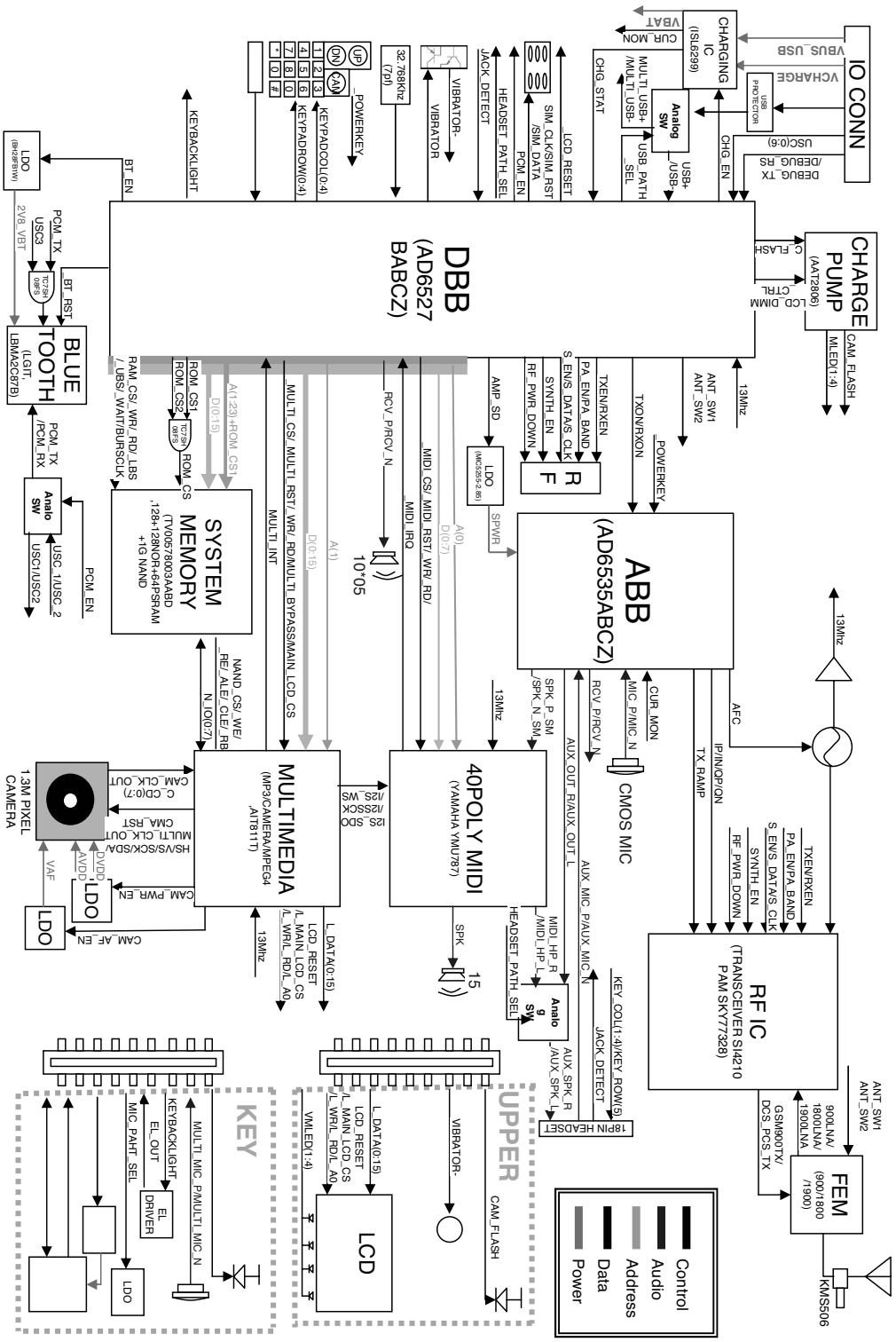
5. DOWNLOAD AND CALIBRATION

9. Press START to execute download

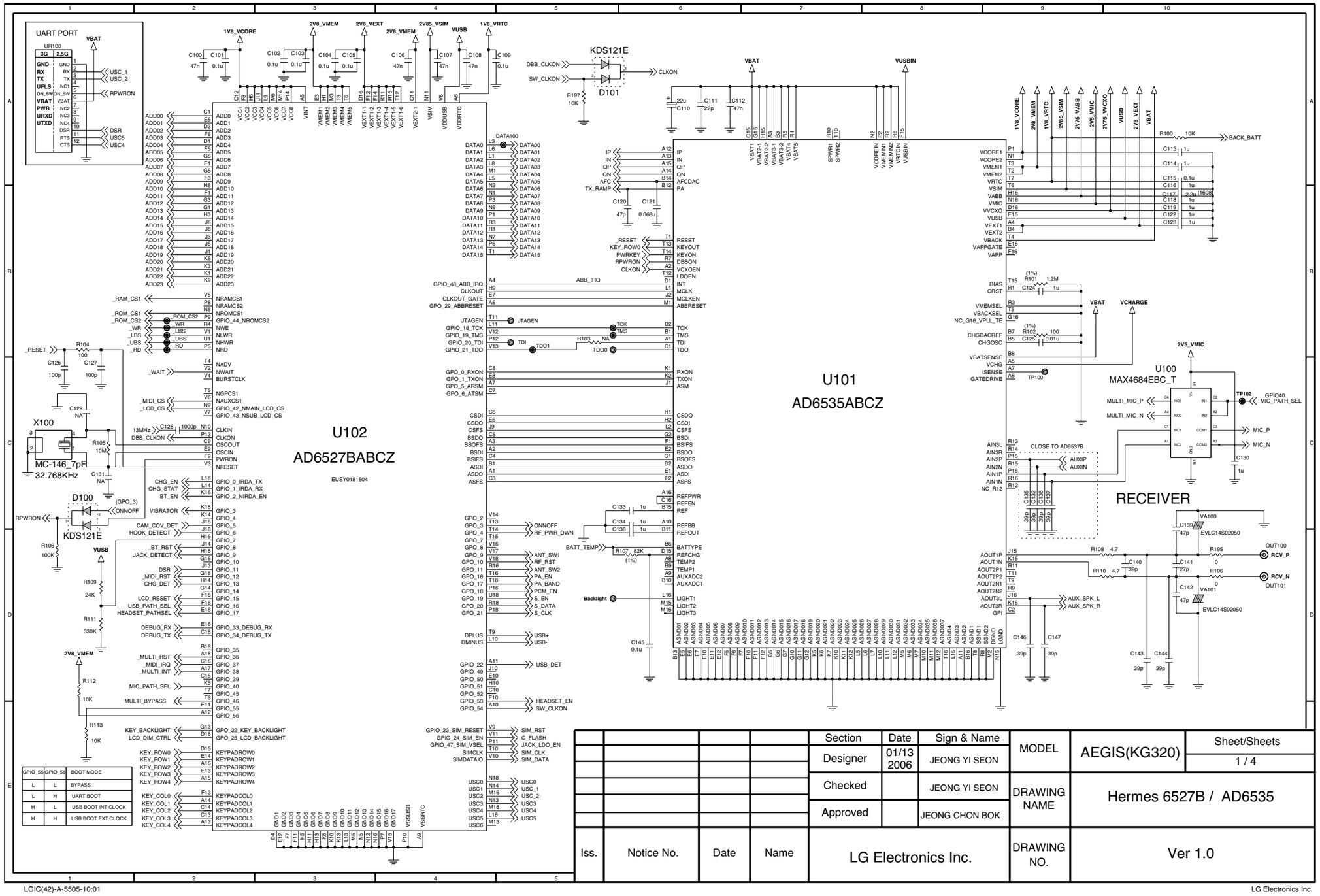
10. Once downloading is started, press STOP button to keep from re-downloading after downloading is completed.



6. BLOCK DIAGRAM

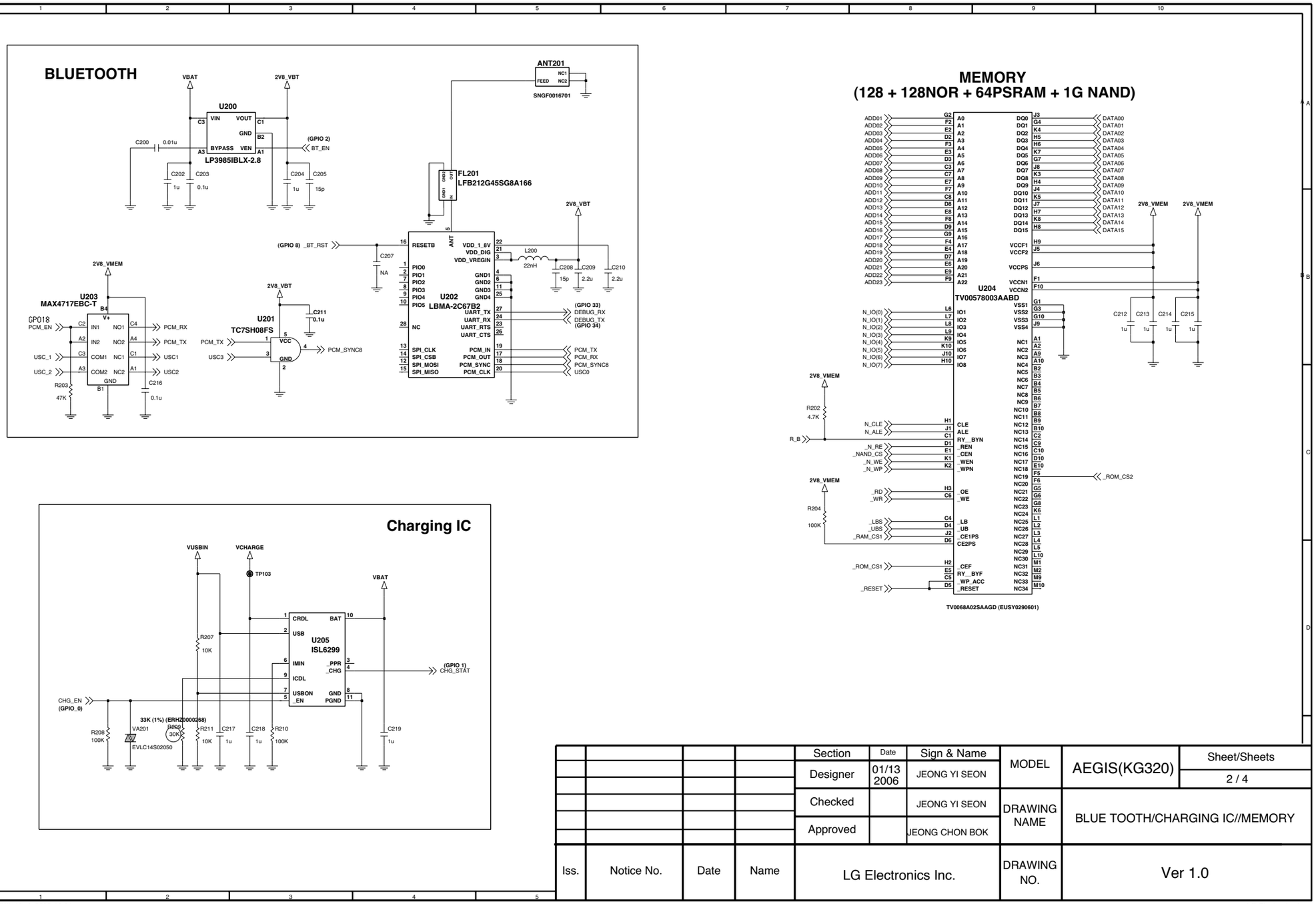


7. CIRCUIT DIAGRAM



				Section	Date	Sign & Name	MODEL	AEGIS(KG320)	Sheet/Sheets
				Designer	01/13 2006	JEONG YI SEON			1 / 4
				Checked		JEONG YI SEON	DRAWING NAME	Hermes 6527B / AD6535	
				Approved		JEONG CHON BOK			
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	Ver 1.0	

7. CIRCUIT DIAGRAM

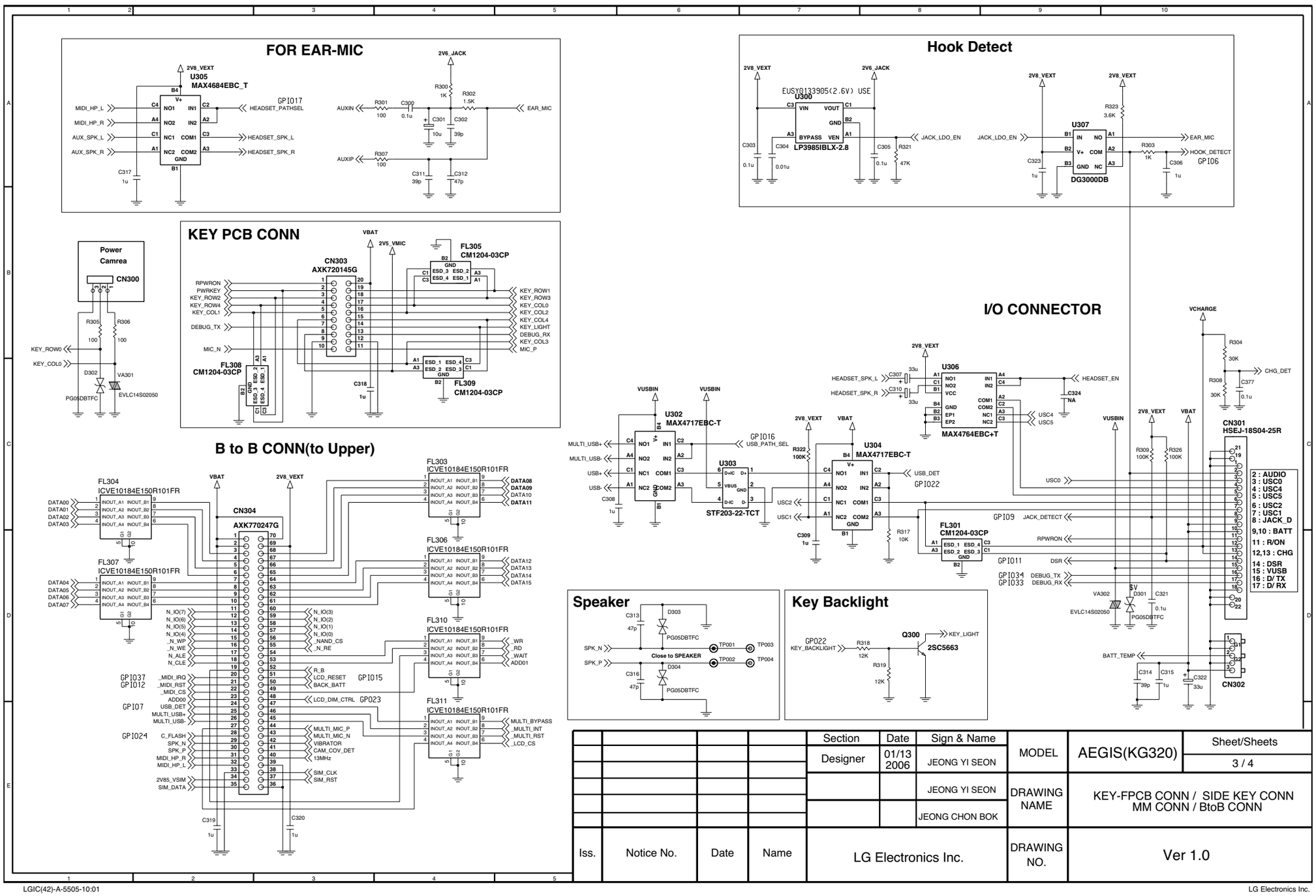


				Section	Date	Sign & Name	MODEL	AEGIS(KG320)	Sheet/Sheets
				Designer	01/13 2006	JEONG YI SEON			2 / 4
				Checked		JEONG YI SEON	DRAWING NAME	BLUE TOOTH/CHARGING IC//MEMORY	
				Approved		JEONG CHON BOK			
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	Ver 1.0	

LGIC(42)-A-5505-10:01

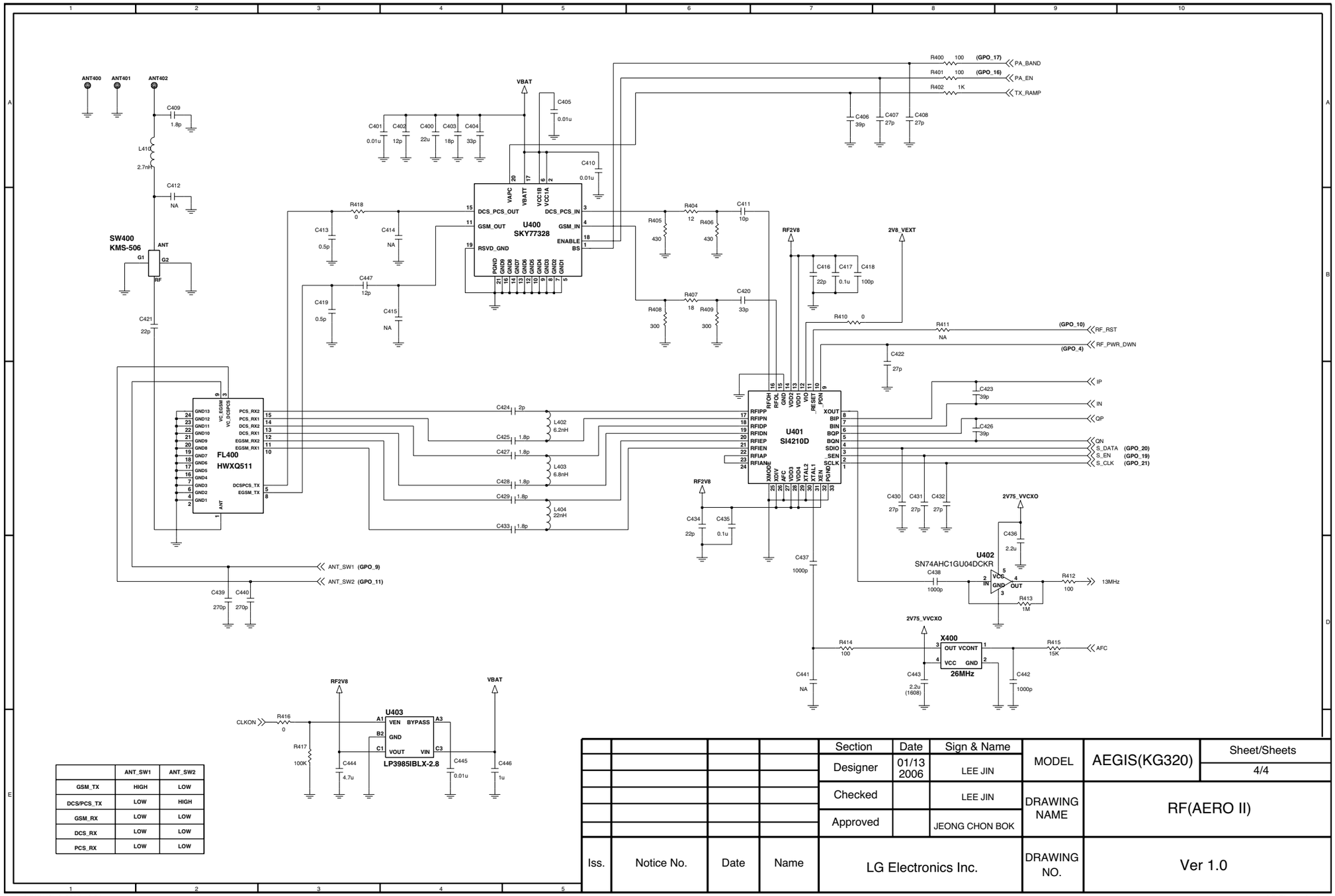
LG Electronics Inc.

7. CIRCUIT DIAGRAM



				Section	Date	Sign & Name	MODEL	AEGIS(KG320)	Sheet/Sheets
				Designer	01/13 2006	JEONG YI SEON			3 / 4
						JEONG YI SEON	DRAWING NAME	KEY-FPCB CONN / SIDE KEY CONN MM CONN / BtoB CONN	
						JEONG CHON BOK			
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	Ver 1.0	

7. CIRCUIT DIAGRAM



	ANT_SW1	ANT_SW2
GSM_TX	HIGH	LOW
DCS/PCS_TX	LOW	HIGH
GSM_RX	LOW	LOW
DCS_RX	LOW	LOW
PCS_RX	LOW	LOW

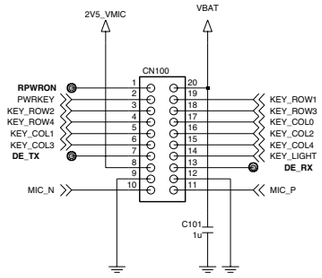
Iss.	Notice No.	Date	Name	Section	Date	Sign & Name	MODEL	AEGIS(KG320)	Sheet/Sheets
				Designer	01/13 2006	LEE JIN			4/4
				Checked		LEE JIN	DRAWING NAME	RF(AERO II)	
				Approved		JEONG CHON BOK			
				LG Electronics Inc.			DRAWING NO.	Ver 1.0	

LGIC(42)-A-5505-10:01

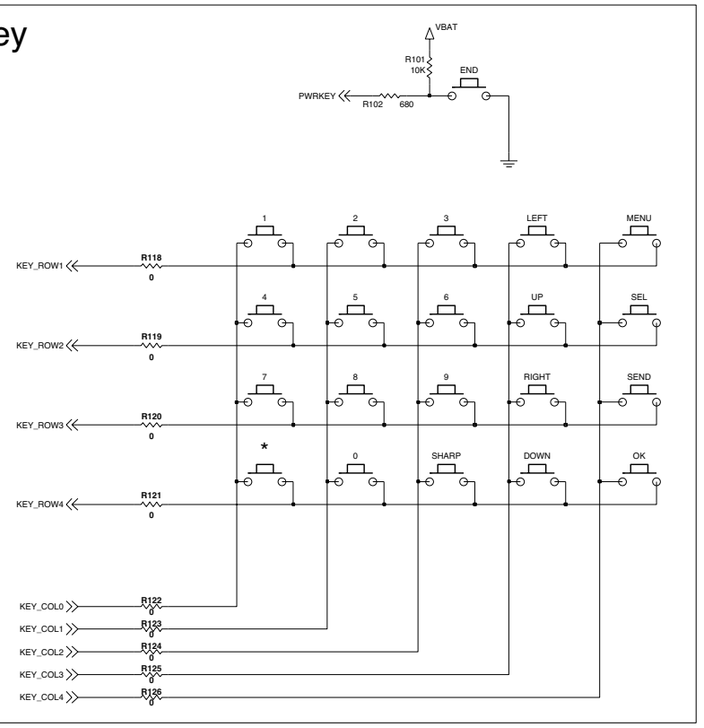
LG Electronics Inc.

7. CIRCUIT DIAGRAM

KEY PCB CONN

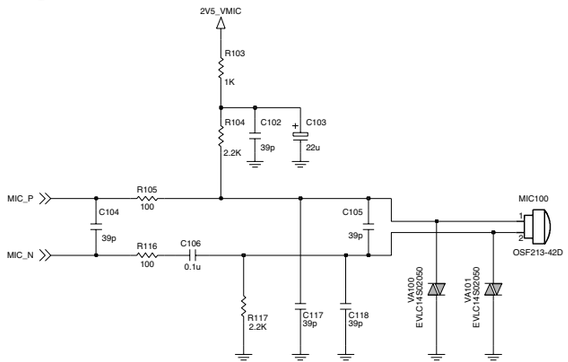


Key

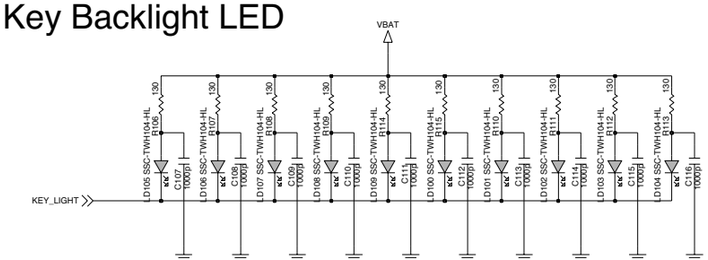


MIC

CLOSE TO MIC



Key Backlight LED



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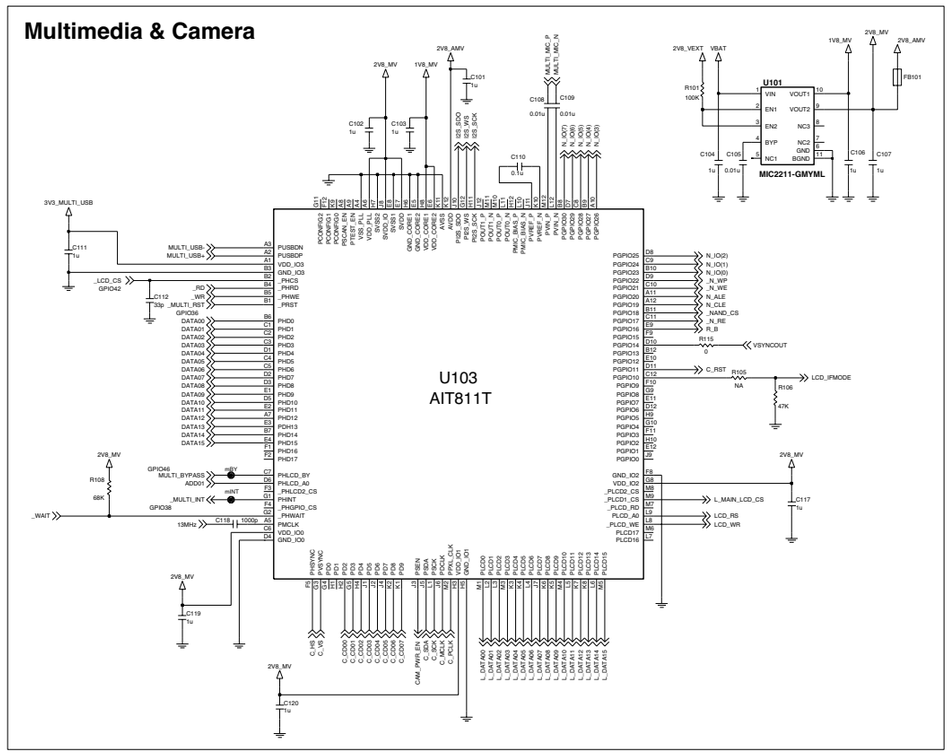
				Checked	2006	JEONG YI SEON	DRAWING NAME	KEY-FPCB KEY-FPCB(KEY, KEY-BACKLIGHT, MIC)	
				Approved	2006	JEONG CHON BOK			
				LG Electronics Inc.			DRAWING NO.	Ver 1.0 LG Electronics Inc.	

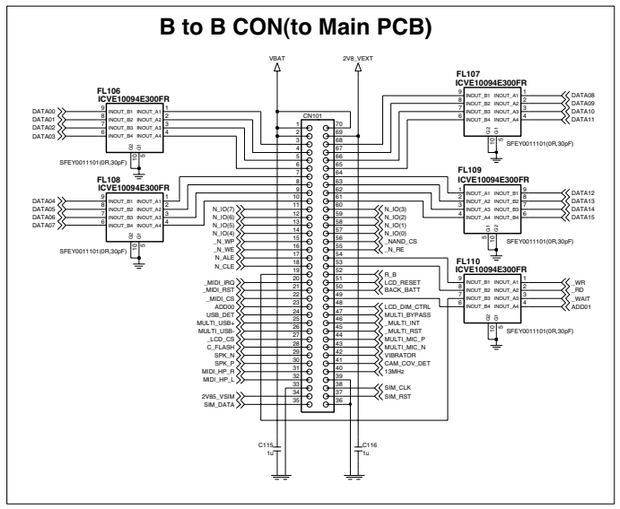
LGIC(42)-A-5505-10:01

7. CIRCUIT DIAGRAM

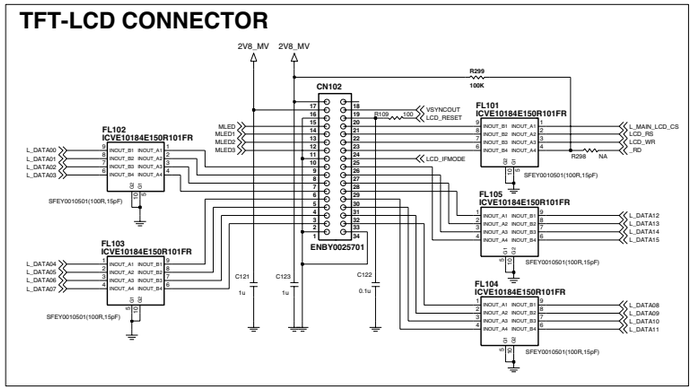
Multimedia & Camera



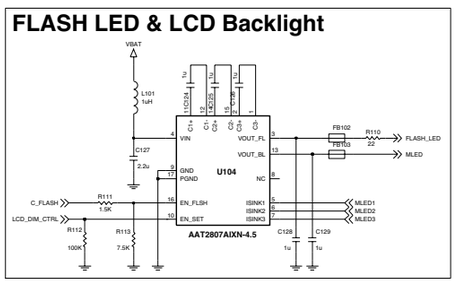
B to B CON(to Main PCB)



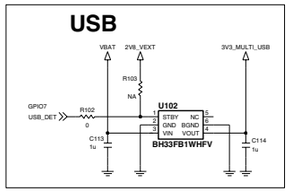
TFT-LCD CONNECTOR



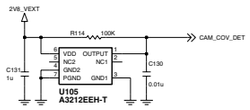
FLASH LED & LCD Backlight



USB



FLIP SWITCH



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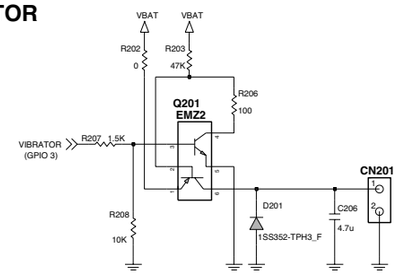
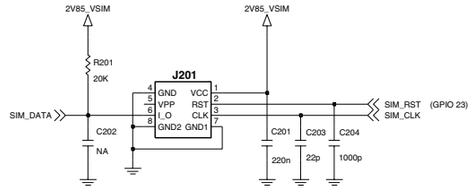
				Checked		JEONG YI SEON	DRAWING NAME	UPPER-ADI	
				Approved		JEONG CHON BOK			
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	Ver 1.0	

7. CIRCUIT DIAGRAM

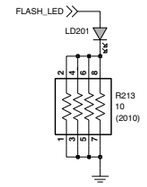
VIBRATOR



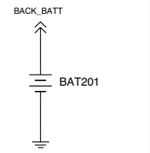
SIM CONNECTOR



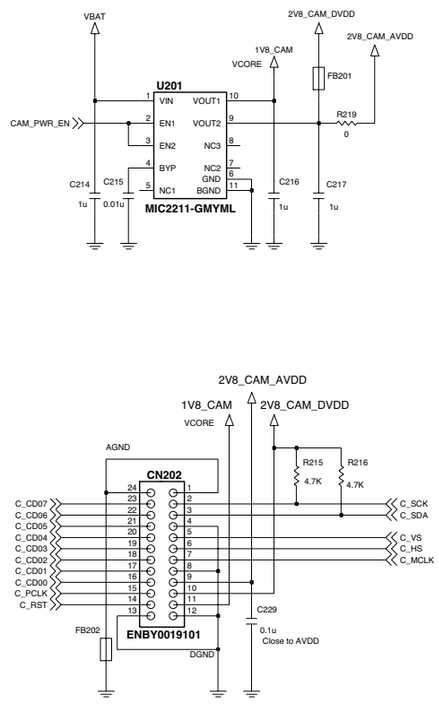
CAMERA FLASH LED



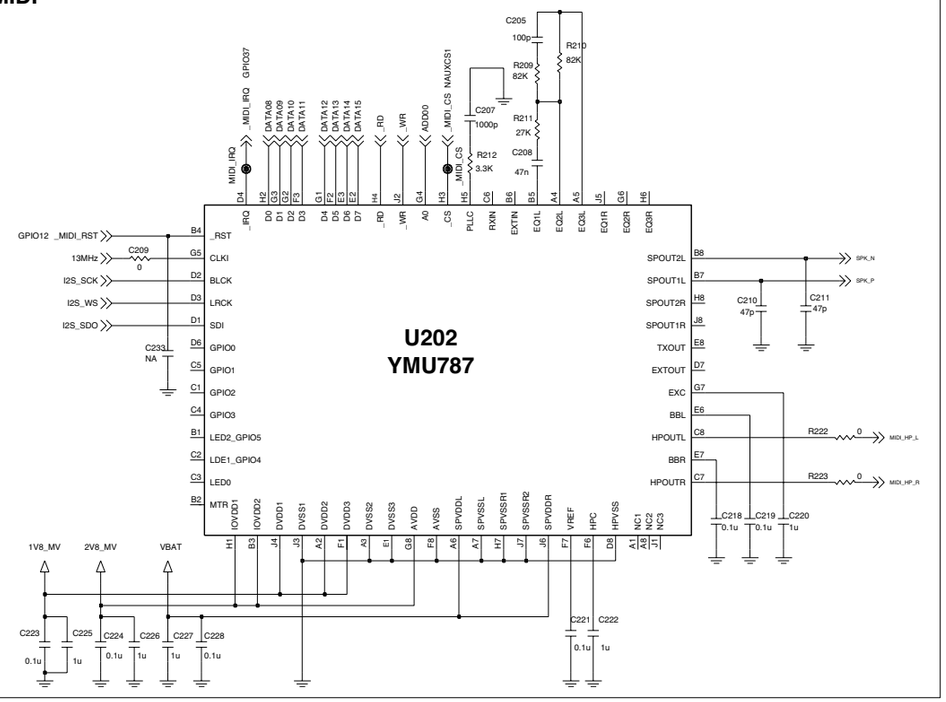
Back-up Battery



1.3M Pixel CAMERA



MIDI



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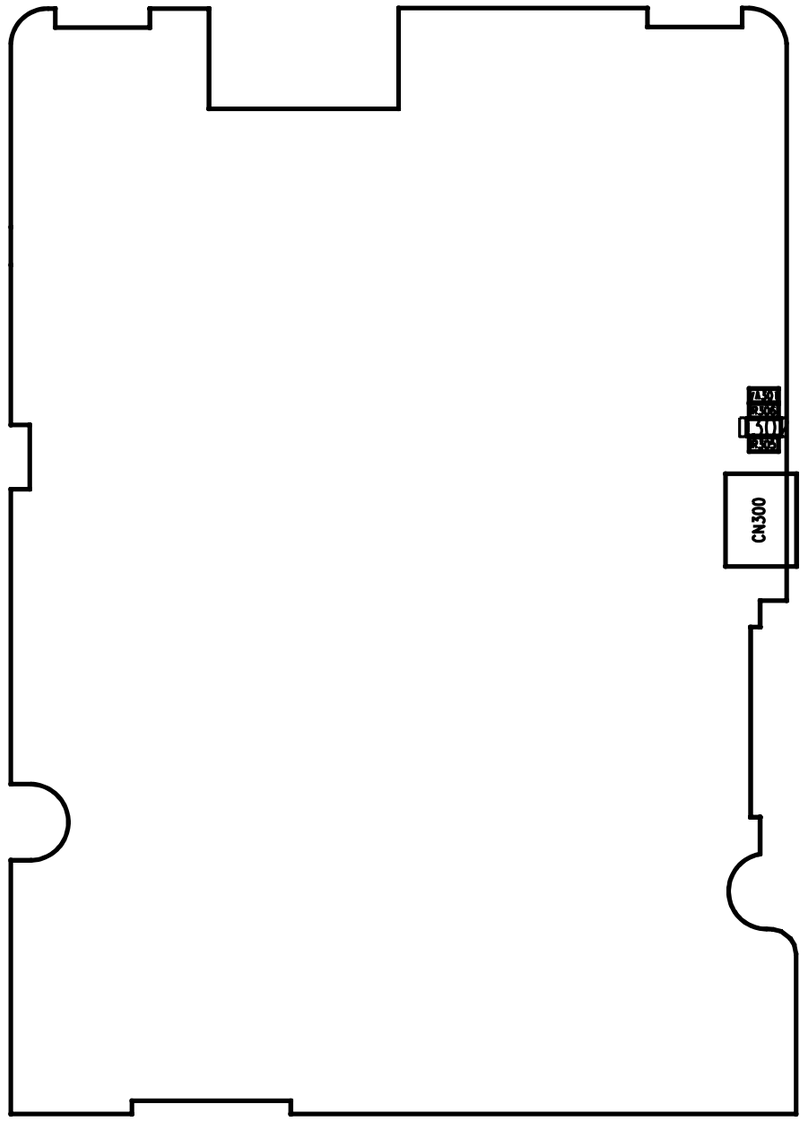
				Checked		JEONG YI SEON	DRAWING NAME	UPPER-ADI	
				Approved		JEONG CHON BOK			
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	Ver 1.0	

LGIC(42)-A-5505-10:01

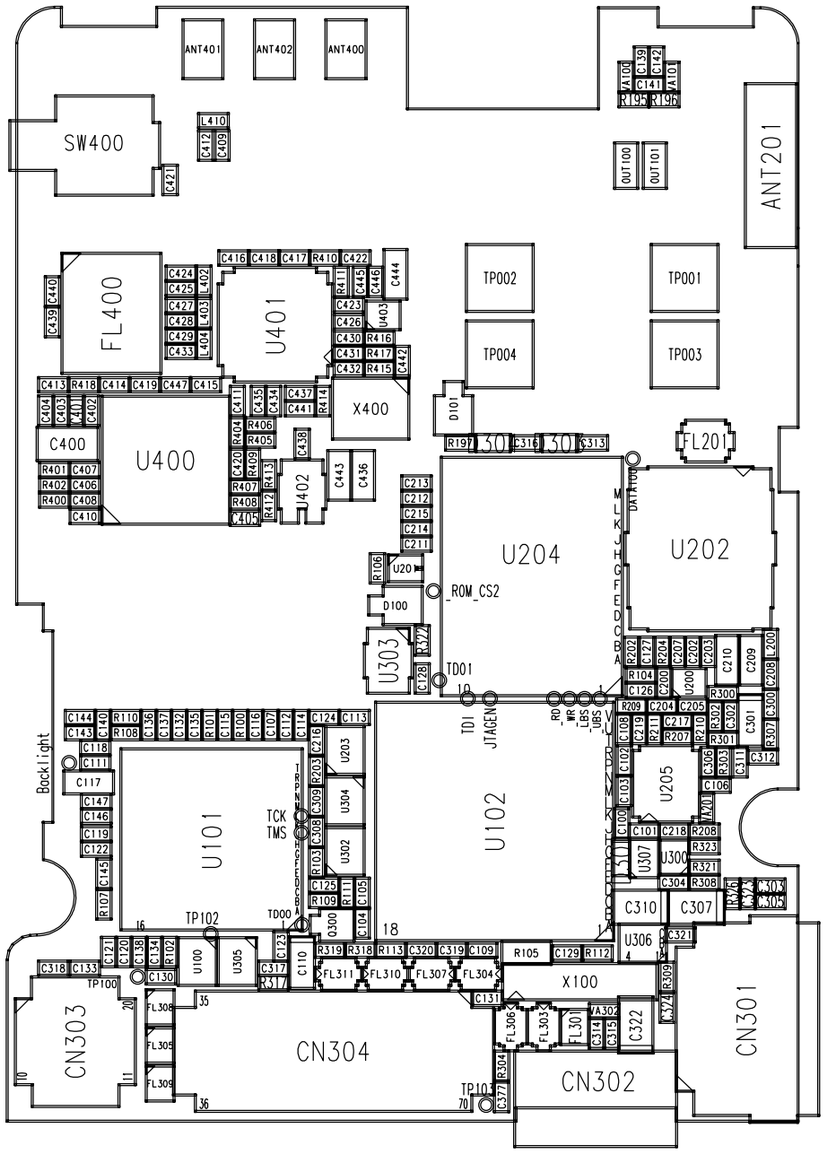
LG Electronics Inc.

8. PCB LAYOUT



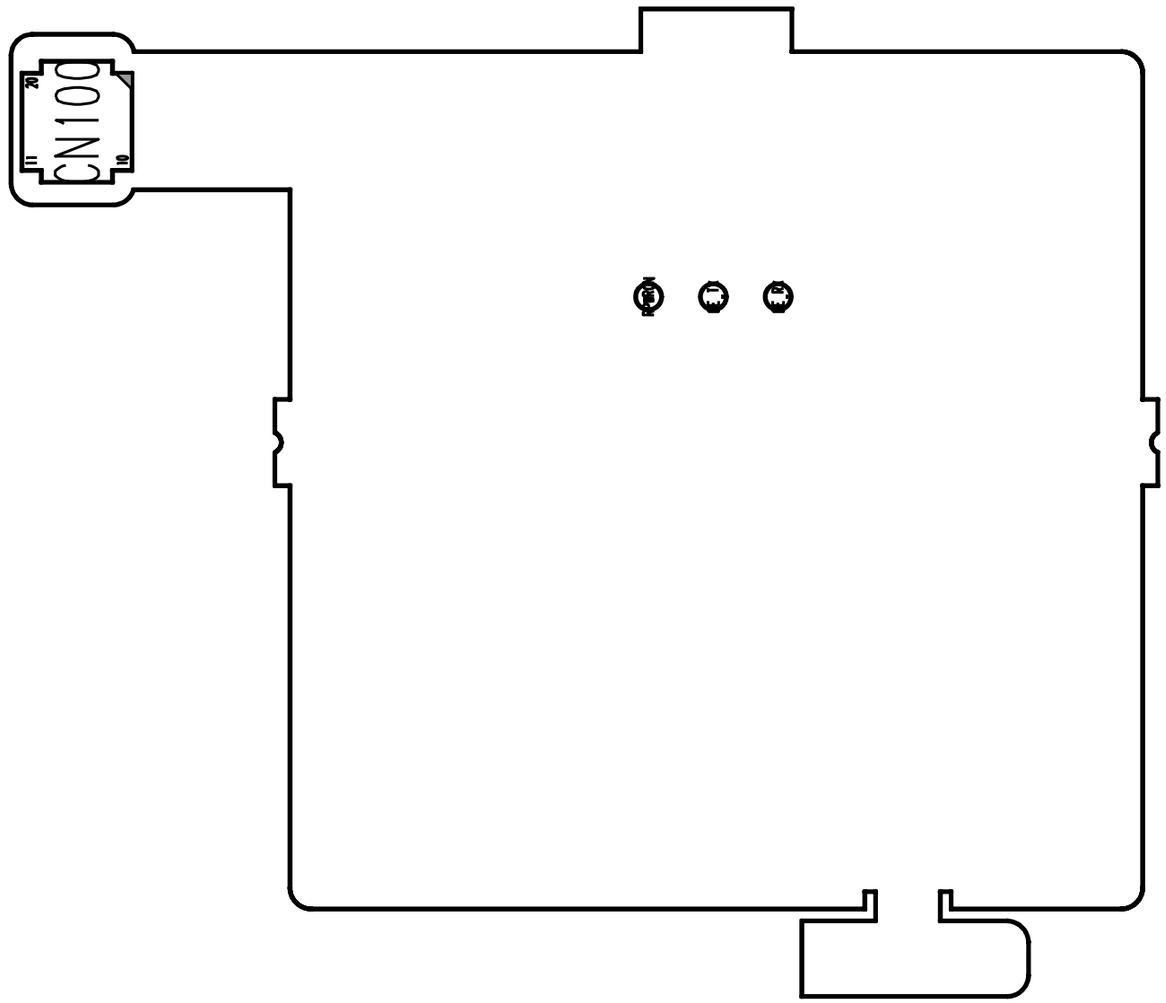
KG320-MAIN-SPFY0122501-1.0-TOP

8. PCB LAYOUT



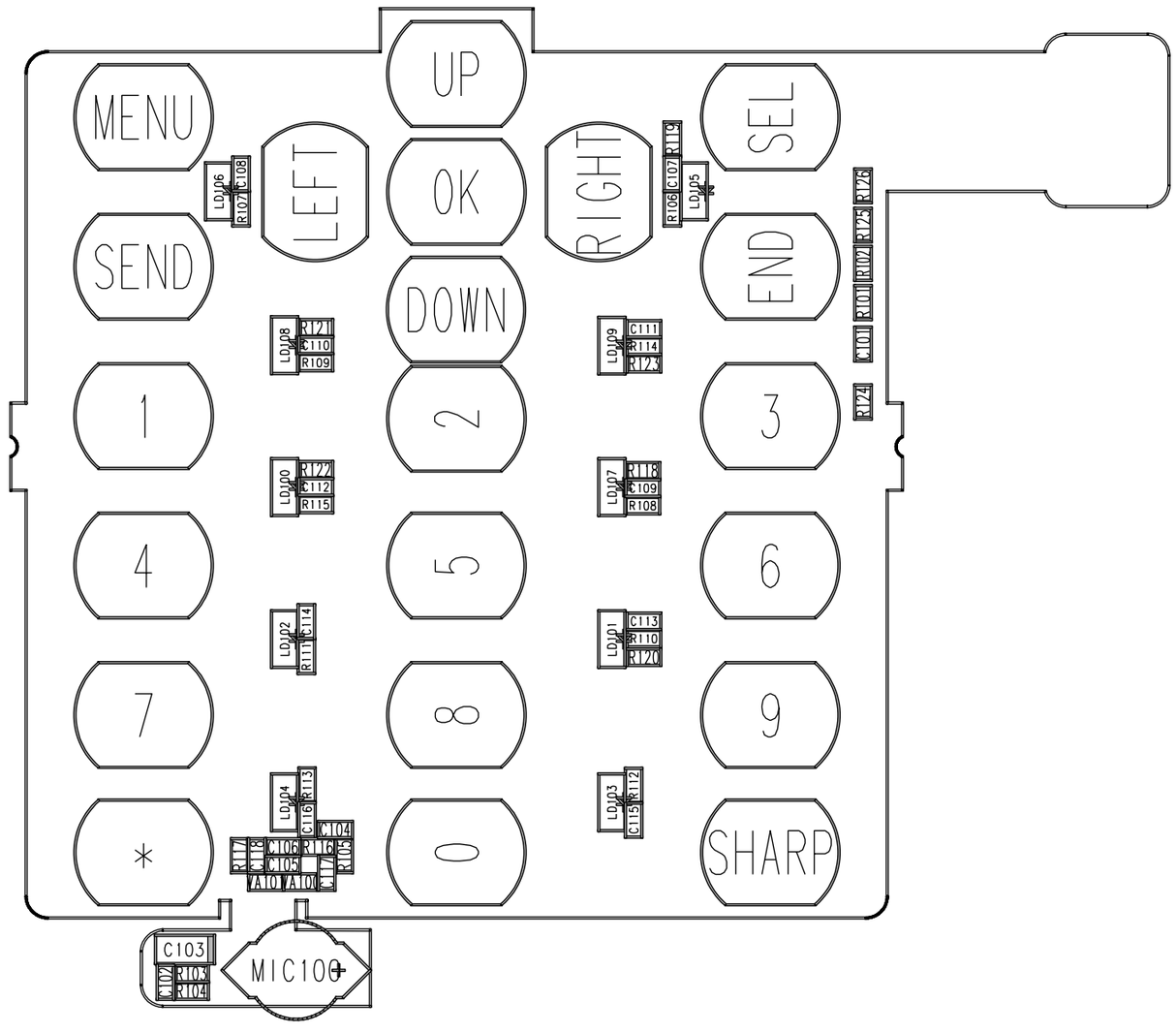
KG320-MAIN-SPFY0122501-1.0-BTM

8. PCB LAYOUT



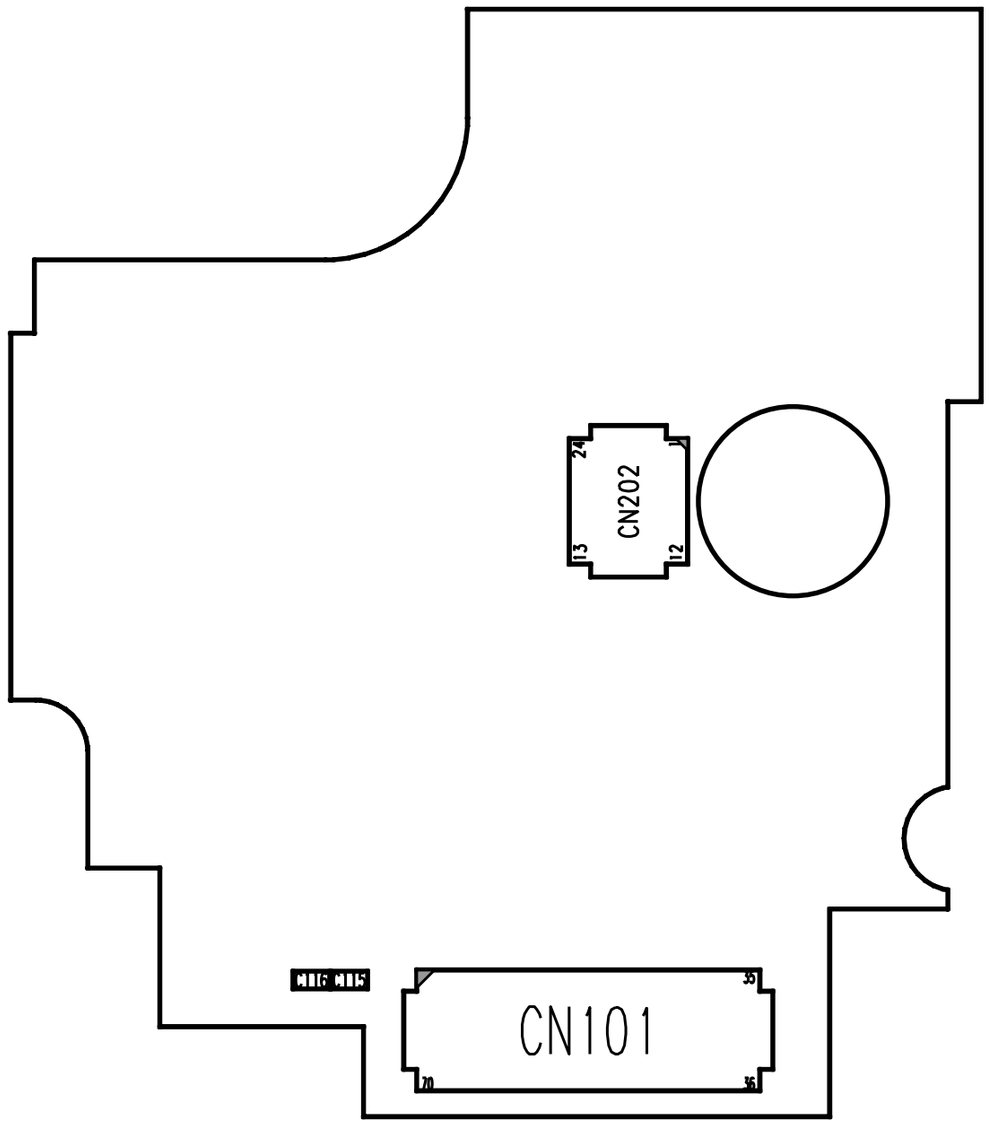
KG320-KEY-FPCB-SPCY0069801-1.0-TOP

8. PCB LAYOUT



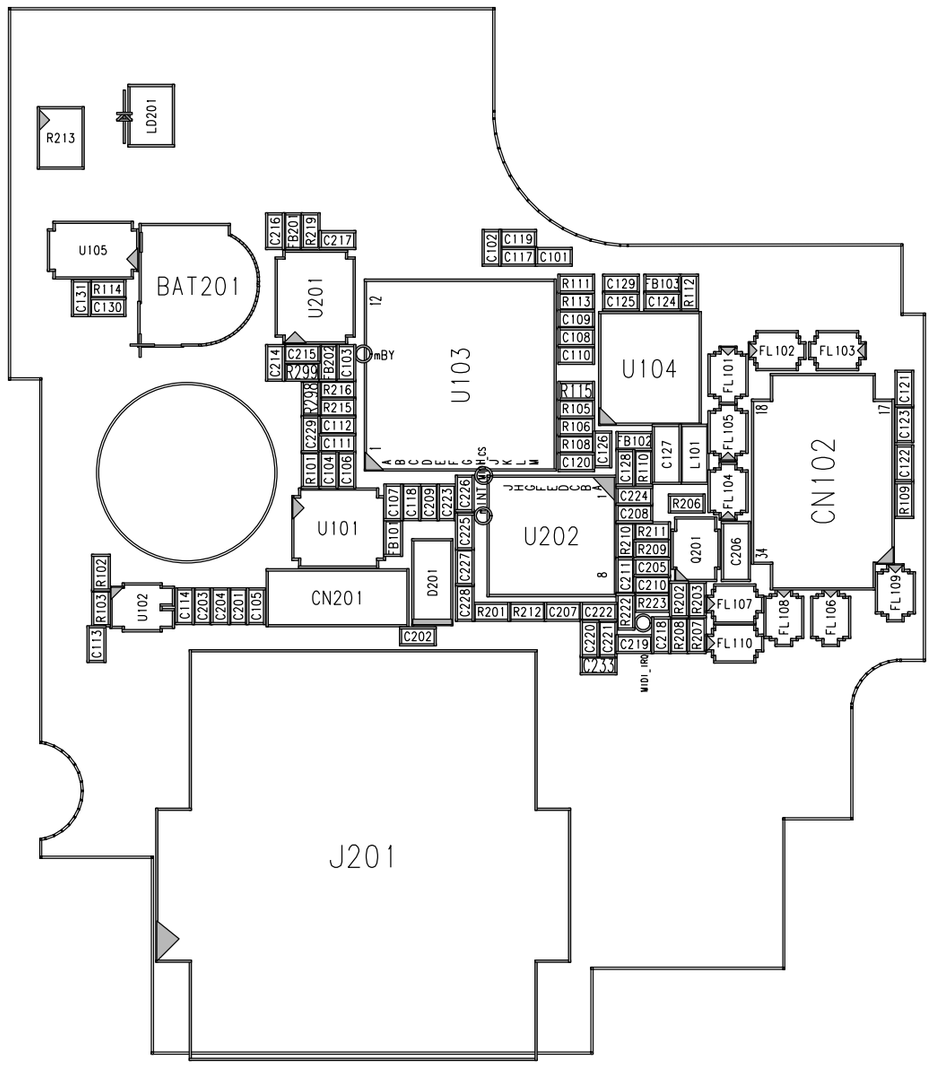
KG320-KEY-FPCB-SPCY0069801-1.0-BTM

8. PCB LAYOUT



KG320-UPPER-SPJY0024301-1.0-TOP

8. PCB LAYOUT



KG320-UPPER-SPJY0024301-1.0-BTM

9. ENGINEERING MODE

A. About Engineering Mode

Engineering mode is designed to allow a service man/engineer to view and test the basic functions provided by a handset.

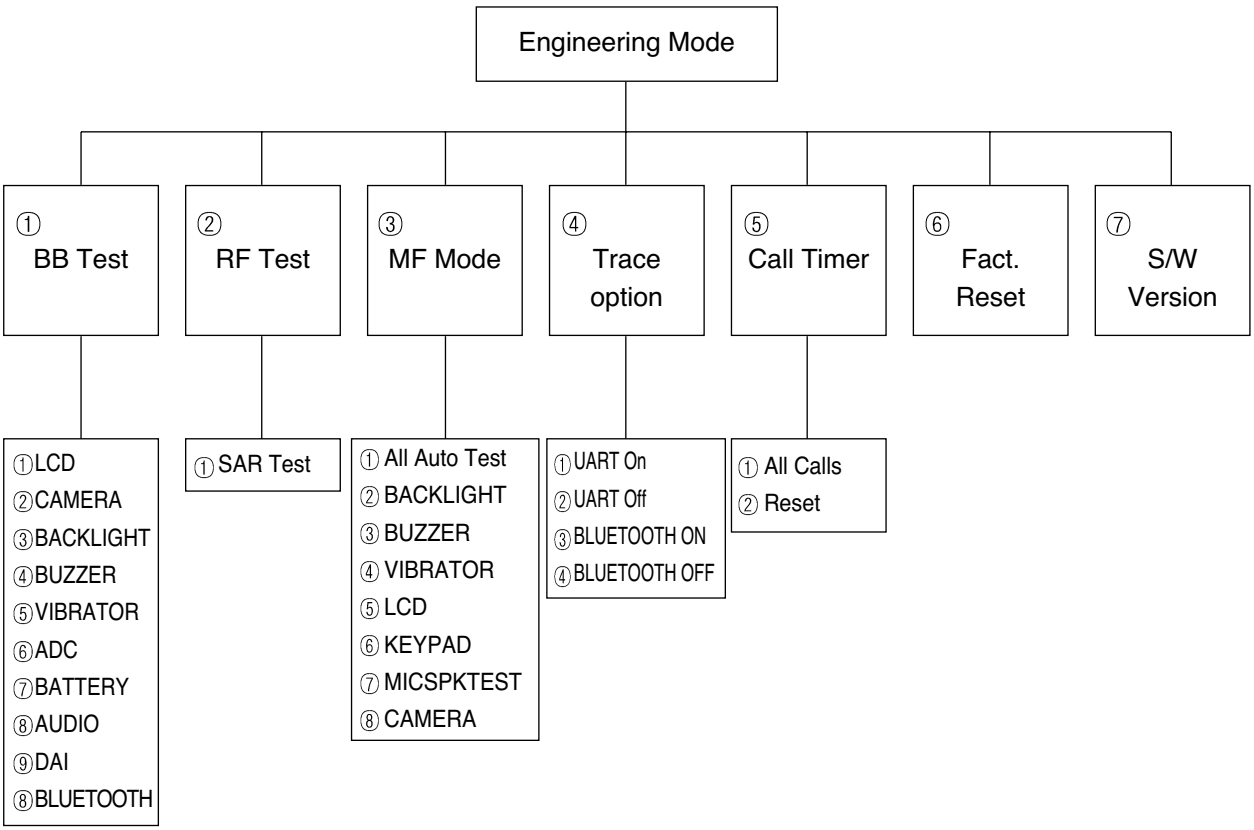
B. Access Codes

The key sequence for switching the engineering mode on is 2945#*#. Pressing END will switch back to non-engineering mode operation.

C. Key Operation

Use Up and Down key to select a menu and press ‘select’ key to progress the test. Pressing ‘back’ key will switch back to the original test menu.

D. Engineering Mode Menu Tree



9. ENGINEERING MODE

9.1 BB Test [MENU 1]

9.1.1 LCD

1) COLOUR : WHITE, RED, GREEN, BLUE, BLACK

9.1.2 CAMERA

This menu is to test the Camera.
1) Main LCD preview : It shows the picture on Main LCD.
2) Flash on : It turns on the Flash LED.
3) Flash off : It turns off the Flash LED.

9.1.3 Backlight

1) Backlight on : LCD Backlight and Keypad EL Backlight light on at the same time.
2) Backlight off : LCD Backlight and Keypad EL Backlight light off at the same time.
3) Backlight value : This controls brightness of Backlight. When entering into the menu, the present backlight-value in the phone is displayed. Use Left/Right key to adjust the level of brightness. The value of the brightness set at last will be saved in the NVRAM.

9.1.4 Buzzer

This menu is to test the melody sound.
1) Melody on : Melody sound is played through the speaker.
2) Melody off : Melody sound is off.

9.1.5 Vibrator

This menu is to test the vibration mode.
1) Vibrator on : Vibration mode is on.
2) Vibrator off : Vibration mode is off.

9.1.6 ADC (Analog to Digital Converter)

This displays the value of each ADC.
1) MVBAT ADC : Main Voltage Battery ADC
2) AUX ADC : Auxiliary ADC
3) TEMPER ADC : Temperature ADC

9.1.7 BATTERY

1) Bat Cal : This displays the value of Battery Calibration. The following menus are displayed in order : BAT_LEV_4V, BAT_LEV_3_LIMIT, BAT_LEV_2_LIMIT, BAT_LEV_1_LIMIT, BAT_IDLE_LI MIT, BAT_INCALL_LIMIT, SHUT_DOWN_VOLTAGE, BAT_RECHARGE_LMT
2) TEMP Cal : This displays the value of Temperature Calibration. The following menus are displayed in order : TEMP_HIGH_LIMIT, TEMP_HIGH_RECHARGE_LMT, TEMP_LOW_RECHARGE_LMT, TEMP_LOW_LIMIT

9.1.8 Audio

This is a menu for setting the control register of Voiceband Baseband Codec chip.
Although the actual value can be written over, it returns to default value after switching off and on the phone.
1) VbControl1 : VbControl1 bit Register Value Setting
2) VbControl2 : VbControl2 bit Register Value Setting
3) VbControl3 : VbControl3 bit Register Value Setting
4) VbControl4 : VbControl4 bit Register Value Setting
5) VbControl5 : VbControl5 bit Register Value Setting
6) VbControl6 : VbControl6 bit Register Value Setting

9.1.9 DAI (Digital Audio Interface)

This menu is to set the Digital Audio Interface Mode for Speech Transcoder and Acoustic testing.
1) DAI AUDIO : DAI audio mode
2) DAI UPLINK : Speech encoder test
3) DAI DOWNLINK : Speech decoder test
4) DAI OFF : DAI mode off

9.1.9 Bluetooth

This menu is to test Bluetooth.
1) Enter test mode
2) Bypass mode On
3) Bypass mode Off

9.2 RF Test [MENU 2]

9.2.1 SAR test

This menu is to test the Specific Absorption Rate.
1) SAR test on : Phone continuously process TX only. Call-setup equipment is not required.
2) SAR test off : TX process off

9.3 MF mode [MENU 3]

This manufacturing mode is designed to do the baseband test automatically. Selecting this menu will process the test automatically, and phone displays the previous menu after completing the test.

9.3.1 All auto test

LCD, Backlight, Vibrator, Buzzer, Key Pad, Mic&Speaker,

9.3.2 Backlight

LCD Backlight is on for about 1.5 seconds at the same time, then off.

9.3.3 Buzzer

This menu is to test the volume of Melody. It rings in the following sequence. Volume 1, Volume 2, Volume 3, Volume 0 (mute), Volume 4, Volume 5.

9.3.4 Vibrator

Vibrator is on for about 1.5 seconds.

9.3.5 LCD

1)LCD
Main LCD screen resolution tests horizontally and vertically one by one and fills the screen.

9.3.6 Key pad

When a pop-up message shows ‘Press Any Key’, you may press any keys including side keys, but not [Soft2 Key]. If the key is working properly, name of the key is displayed on the screen. Test will be completed in 15 seconds automatically.

9.3.7 MicSpk Test

The sound from MIC is recorded for about 3 seconds, then it is replayed on the speaker automatically.

9.4 Trace option [MENU 4]

This is NOT a necessary menu to be used by neither engineers nor users.

9.5 Call timer [MENU 5]

This menu is to set the Digital Audio Interface Mode for Speech Transcoder and Acoustic testing.
1) All calls : This displays total conversation time. User cannot reset this value.
2) Reset settings : This resets total conversation time to this, [00:00:00].
3) DAI DOWNLINK : Speech decoder test
4) DAI OFF : DAI mode off

9.6 Fact. Reset [MENU 6]

This Factory Reset menu is to format data block in the flash memory and this procedure set up the default value in data block.

Attention
① Fact. Reset (i.e.Factory Reset) should be only used during the Manufacturing process.
② Servicemen should NOT progress this menu, otherwise some of valuable data such as Setting value, RF Calibration data, etc. cannot be restored again.

9.7 S/W version

This displays software version stored in the phone.

10. STAND ALONE TEST

10.1 Introduction

This manual explains how to examine the status of RX and TX of the model.

A. Tx Test

TX test - this is to see if the transmitter of the phones is activating normally.

B. Rx Test

RX test - this is to see if the receiver of the phones is activating normally.

10.2 Setting Method

A. COM port

a. Move your mouse on the “Connect” button, then click the right button of the mouse and select “Com setting”.
b. In the “Dialog Menu”, select the values as explained below.
- Port : select a correct COM port
- Baud rate : 38400
- Leave the rest as default values

B. Tx

1. Selecting Channel
- Select one of GSM or DCS Band and input appropriate channel.

2. Selecting APC
a. Select either Power level or Scaling Factor.
b. Power level
- Input appropriate value GSM (between 5~19) or DCS (between 0~15)

c. Scaling Factor
- A ‘Ramp Factor’ appears on the screen.
- You may adjust the shape of the Ramp or directly input the values.

C. Rx

1. Selecting Channel
- Select one of GSM or DCS Band and input appropriate channel.

2. Gain Control Index (0~ 26) and RSSI level
- See if the value of RSSI is close to -16dBm when setting the value between 0 ~ 26 in Gain Control Index.
- Normal phone should indicate the value of RSSI close to -16dBm.

10.3 Means of Test

a. Select a COM port
b. Set the values in Tx or Rx
c. Select band and channel
d. After setting them all above, press connect button.
e. Press the start button

Figure 10-1. HW test program

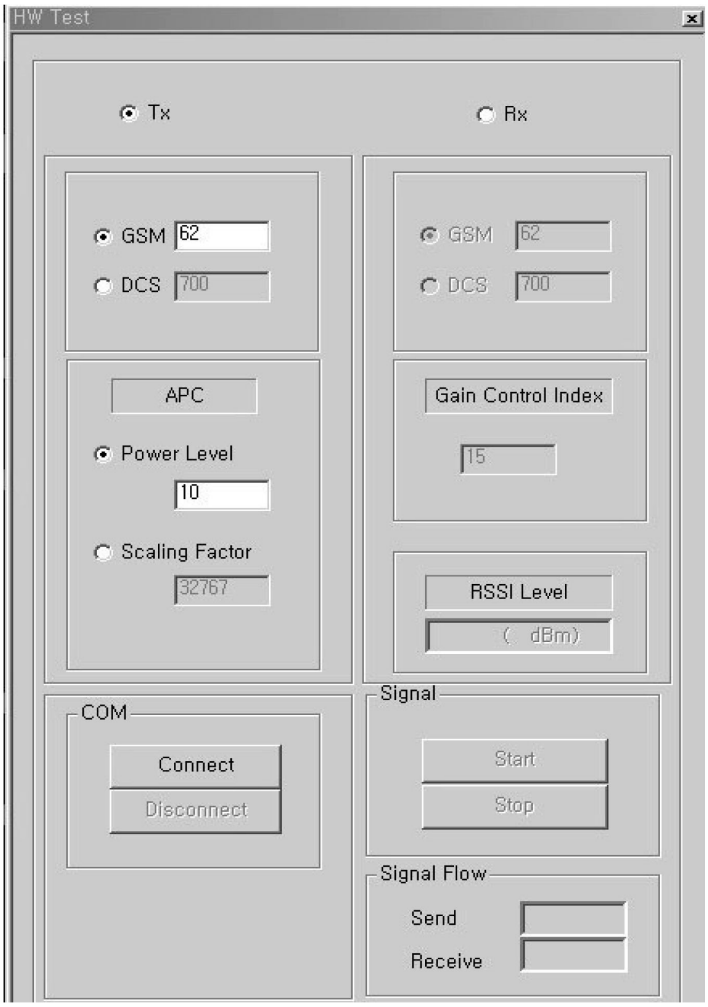


Figure 10-2. HW test setting

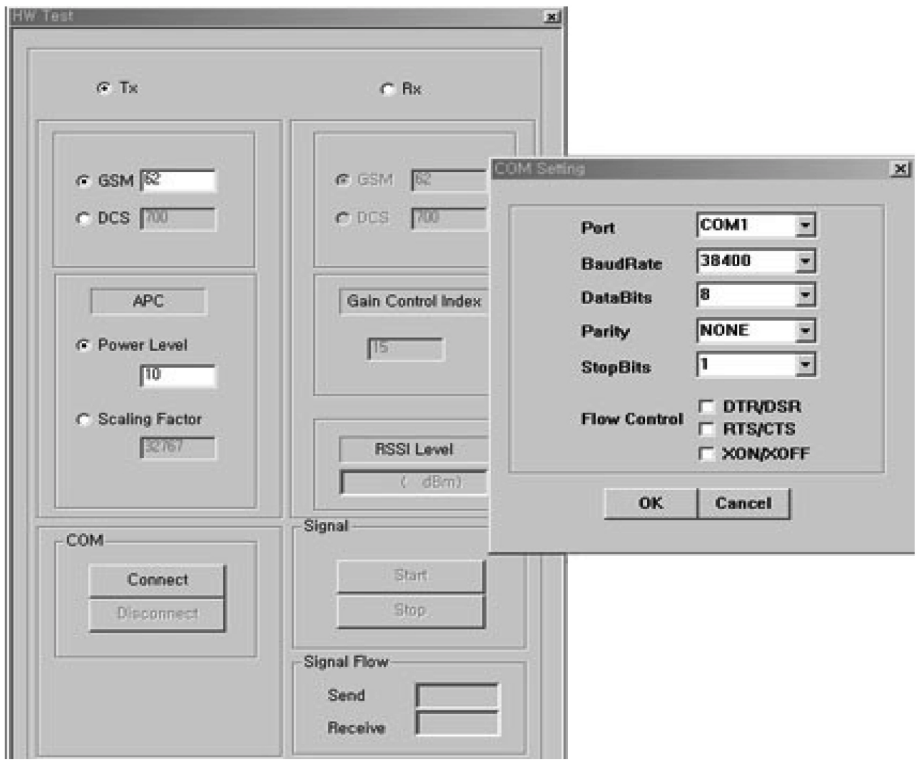
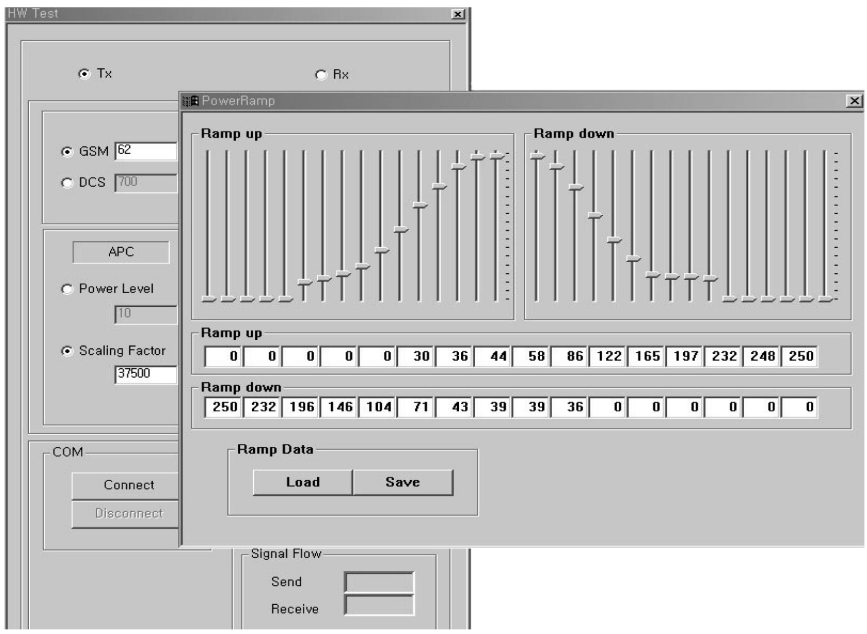


Figure 10-3. Ramping profile



11. AUTO CALIBRATION

11.1 Calibration

A. Overview

Auto-cal (Auto Calibration) is the PC side Calibration tool that perform Tx, Rx and Battery Calibration with Agilent 8960(GSM call setting instrument) and Tektronix PS2521G(Programmable Power supply). Auto-cal generates calibration data by communicating with phone and measuring equipment then write it into calibration data block of flash memory in GSM phone.

B. Equipment List

Table 11-1. Calibration Equipment List.

Equipment for Calibration	Type / Model	Brand
Wireless Communication Test Set	HP-8960	Agilent
RS-232 Cable and Test JIG		LG
RF Cable		LG
Power Supply	HP-66311B	Agilent
GPIO interface card	HP-GPIB	Agilent
Calibration & Final test software		LG
Test SIM Card		
PC (for Software Installation)	Pentium II class above 300MHz	

C. Equipment Setup

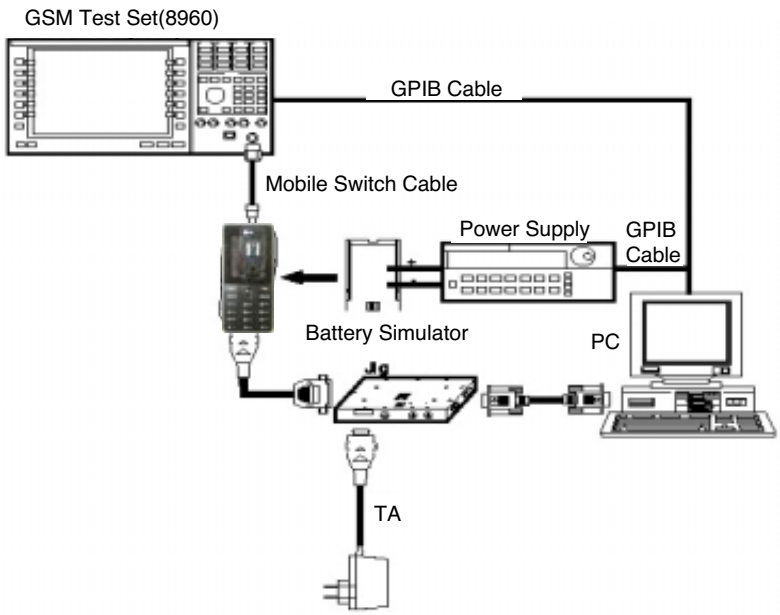


Figure 11-2. Equipment Setup

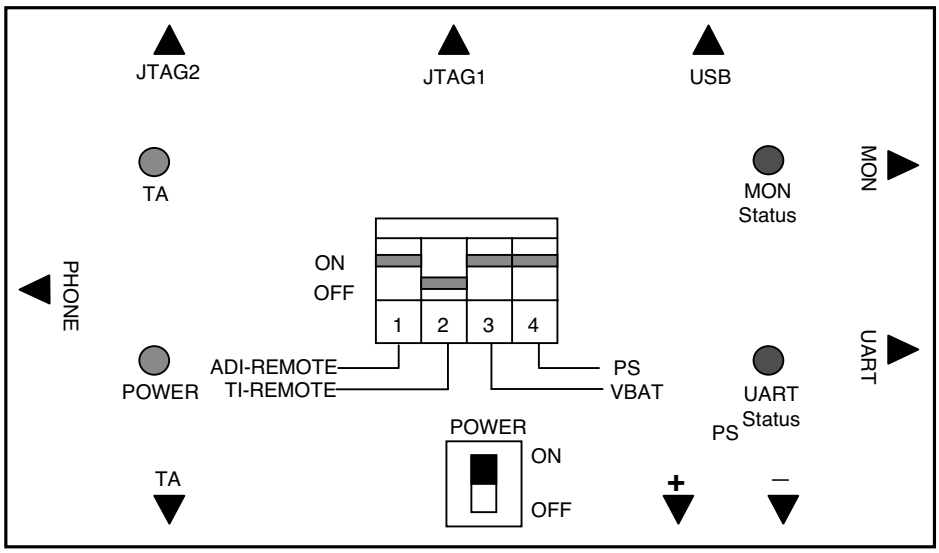


Figure 11-3 The top view of Test JIG

D. Test Jig Operation

Power Source	Description
Power Supply	Usually 4.0V
Travel Adaptor	Use TA, name is TA-20G(24pin)

Table 11-2 Jig Power

Switch Number	Name	Description
Switch 1	ADI-REMOTE	In ON state, phone is awaked. It is used ADI chipset.
Switch 2	TI-REMOTE	In ON state, phone is awaked. It is used TI chipset.
Switch 3	VBAT	Power is provided for phone from battery
Switch 4	PS	Power is provided for phone from Power supply

Table 11-3 Jig DIP Switch

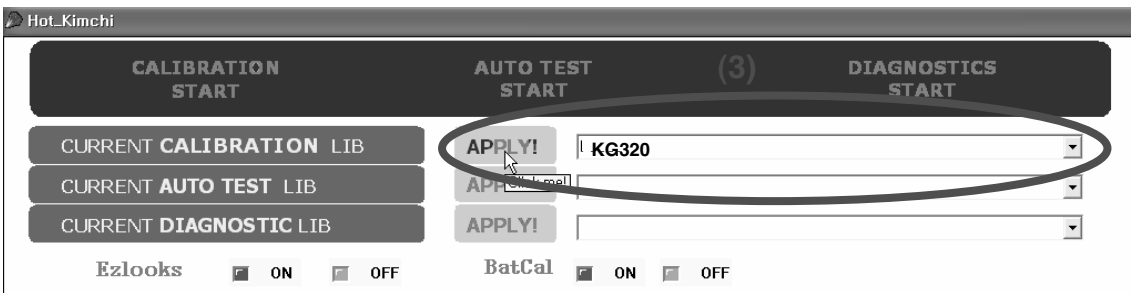
LED Number	Name	Description
LED 1	Power	Power is provided for Test Jig
LED 2	TA	Indicate charging state of the phone battery
LED 3	UART	Indicate data transfer state through the UART port
LED 4	MON	Indicate data transfer state through the MON port

Table 11-4 LED Description

1. Connect as Fig 11-2(RS232 serial cable is connected between COM port of PC and MON port of TEST JIG, in general)
2. Set the Power Supply 4.0V
3. Set the 3rd, 4th of DIP SW ON state always
4. Press the Phone power key, if the Remote ON is used, 1st ON state

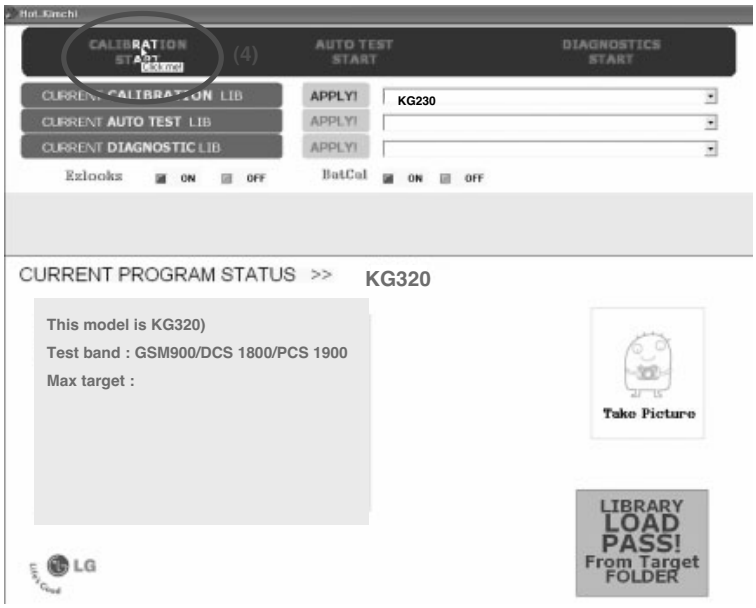
E. Procedure

1. Connect as Fig 11-2 (RS232 serial cable is connected between COM port of PC and MON port of TEST JIG, in general.)
2. Run **Hot_Kimchi.exe** to start calibration.
3. From the Calibration Lib menu, Select F3000, then, Press APPLY!



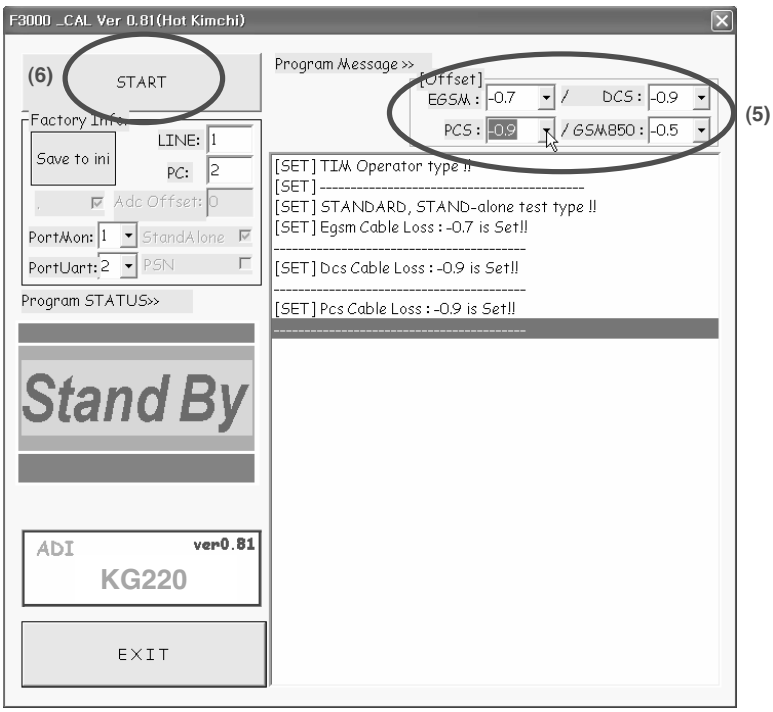
11. AUTO CALIBRATION

4. Press Calibration START



5. Select RF Cable Loss value from the Offset menu

6. Press START to execute calibration



11.2 AGC

This procedure is for Rx calibration.
In this procedure, We can get RSSI correction value. Set band EGSM and press Start button the result window will show correction values per every power level and gain code and the same measure is performed per every frequency.

11.3 APC

This procedure is for Tx calibration.
In this procedure you can get proper scale factor value and measured power level.

11.4 ADC

This procedure is for battery calibration.
You can get main Battery Config Table and temperature Config Table

11.5 Setting

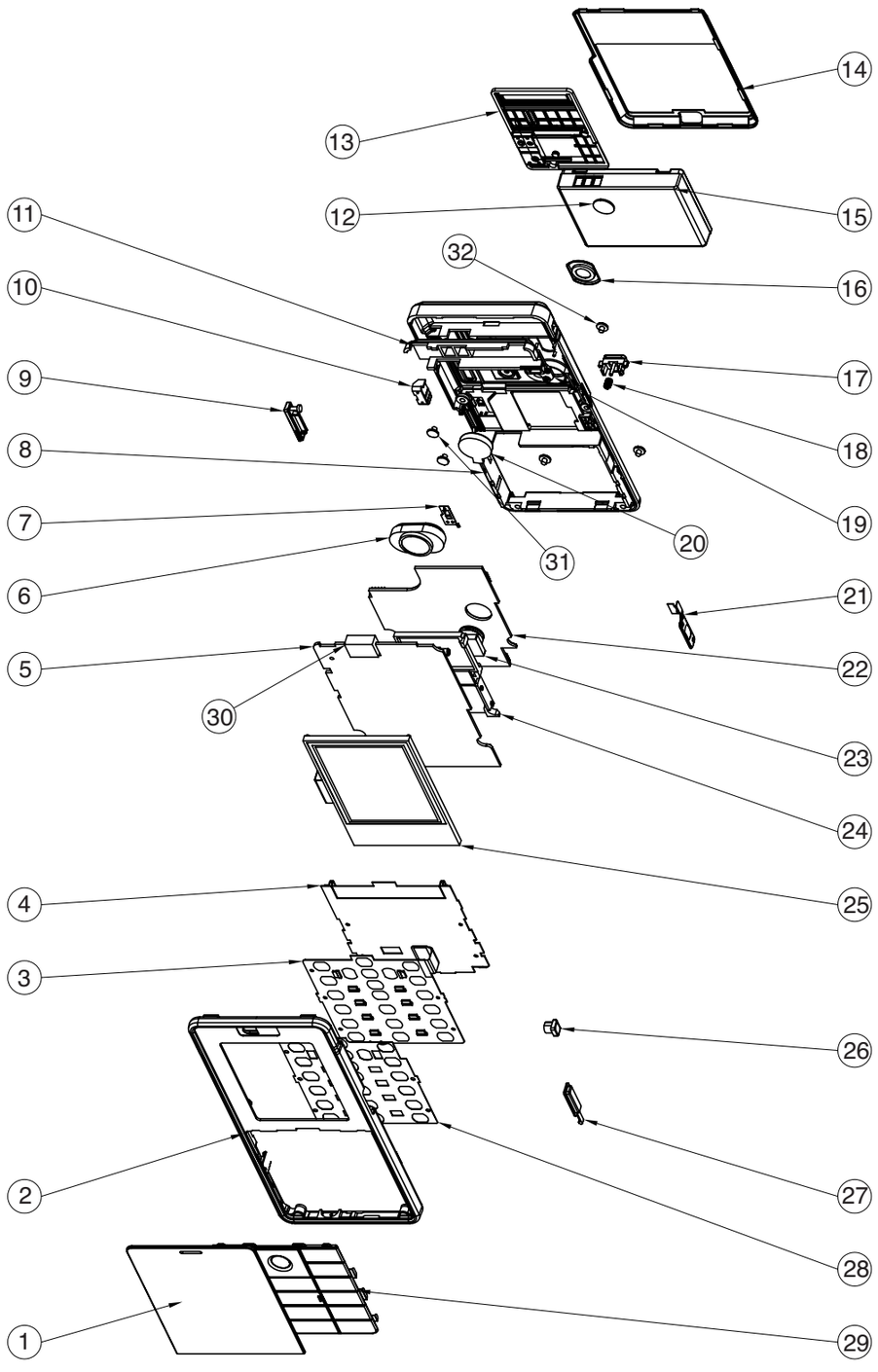
check com port and cable loss. Select automatic calibration item. If you uncheck one item calibration will stop from the unchecked item. This is useful when you want to process only one item.

11.6 How to do calibration

B. Connect Ag8960 equipment and Power Supply and phone.
C. Set correct port and baud rate.
D. Press Start button. AutoCal process all calibration procedure
   i. AGC EGSM
   ii. AGC DCS
   iii. APC EGSM
   iv. APC DCS
   v. ADC
E. After finished all measurement. The state is return to SETUP.
F. The Cal file will be generated and then the calibration data will be written into phone and then will be reset.

12. EXPLODED VIEW & REPLACEMENT PART LIST

12.1 EXPLODED VIEW



No.	DESCRIPTION	Q'TY	PART NO.	REMARK
1	LCD WINDOW	1		
2	COVER FRONT	1		
3	KEY F-PCB	1		
4	SUS BRACKET	1		
5	MAIN PCB	1		
6	SPEAKER	1		
7	SUS GROUND	1		
8	COVER REAR	1		
9	CAP MMI	1		
10	COVER GUIDE	1		
11	ANTENNA	1		
12	WINDOW CAMERA	1		
13	ASSY COVER CAMERA	1		
14	COVER BATTERY	1		
15	BATTERY	1		
16	DECO CAMERA	1		
17	BATTERY LOCKER	1		
18	SPRING	1		
19	WINDOW FLASH	1		
20	VIB-MOTOR	1		
21	CAMERA F-PCB	1		
22	SUB PCB	1		
23	CAMERA MODULE	1		
24	PCB BRACKET	1		
25	LCD MODULE	1		
26	CAP MOBILE SWITCH	1		
27	BUTTON CAMERA	1		
28	METAL DOME ASSY	1		
29	BUTTON DAIL	1		
30	RECEIVER	1		
31	SCREW MACHINE	2		GMZZ0019001
32	SCREW MACHINE	4		GMZZ0017701